Elektronische Bauelemente

SPRD6330S-C

16.2A, 30V, $R_{DS(ON)}$ 6.6mΩ

Dual N-Ch Shielded Gate Trench Power MOSFET

RoHS Compliant Product

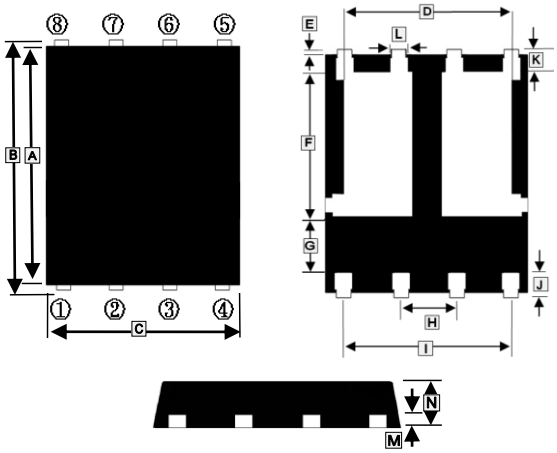
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

The SPRD6330S-C is the Shielded Gate Technology Dual N-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The SPRD6330S-C meet the RoHS and Green Product requirement with full function reliability approved.

DFN5x6-8D



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.70	5.80	H	1.27 BSC.	
B	5.90	6.10	I	3.61	3.96
C	4.80	5.00	J	0.51	0.71
D	3.61	3.96	K	0.41	0.61
E	0.06	0.20	L	0.33	0.51
F	3.38	3.78	M	0.20	0.30
G	1.10	-	N	0.90	1.10

FEATURES

- Shielded Gate Trench Technology
- Super Low Gate Charge
- Green Device Available

MARKING

6330S

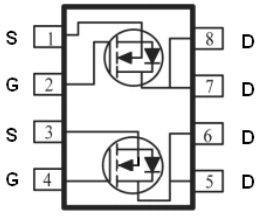
□□□□ ← □=Date Code

PACKAGE INFORMATION

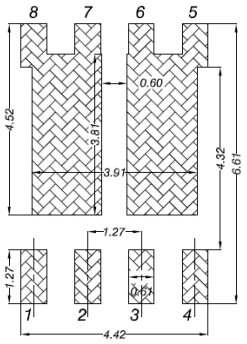
Package	MPQ	Leader Size
DFN5x6-8D	3K	13 inch

ORDER INFORMATION

Part Number	Type
SPRD6330S-C	Lead (Pb)-free and Halogen-free



Mounting Pad Layout



*Dimensions in millimeters

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1] @V_{GS}=10V	T_A=25°C	I_D	16.2	A
	T_A=70°C		13.8	
Pulsed Drain Current [2,3]		I_{DM}	60	A
Total Power Dissipation [1]	T_C=25°C	P_D	23	W
	T_A=25°C		2.9	
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55~150	°C
Thermal Data				
Thermal Resistance Junction-Ambient [1]		$R_{\theta JA}$	t≦10s, 43	°C/W
			Steady State, 62.5	
Thermal Resistance Junction-Case [1]		$R_{\theta JC}$	5.4	

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		BV_{DSS}	30	-	-	V	V_{GS}=0, I_D=250μA
Gate Threshold Voltage		$V_{GS(th)}$	1	-	2.5	V	V_{DS}=V_{GS}, I_D=250μA
Forward Transfer Conductance		g_{fs}	-	67	-	S	V_{DS}=5V, I_D=15A
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current	T_J=25°C	I_{DSS}	-	-	1	μA	V_{DS}=24V, V_{GS}=0
	T_J=55°C		-	-	5		
Static Drain-Source On-Resistance [3]		$R_{DS(ON)}$	-	4.9	6.6	mΩ	V_{GS}=10V, I_D=8A
			-	6.9	9.6		V_{GS}=4.5V, I_D=5A
Total Gate Charge		Q_g	-	8	-	nC	I_D=15A V_{DS}=15V V_{GS}=4.5V
Gate-Source Charge		Q_{gs}	-	2.4	-		
Gate-Drain Change		Q_{gd}	-	3.2	-		
Turn-on Delay Time		$T_{d(on)}$	-	7.1	-	nS	V_{DD}=15V I_D=15A V_{GS}=10V R_G=3.3Ω
Rise Time		T_r	-	40	-		
Turn-off Delay Time		$T_{d(off)}$	-	15	-		
Fall Time		T_f	-	6	-		
Input Capacitance		C_{iss}	-	802	-	pF	V_{GS}=0 V_{DS}=25V f=1MHz
Output Capacitance		C_{oss}	-	322	-		
Reverse Transfer Capacitance		C_{rss}	-	17	-		
Source-Drain Diode							
Continuous Source Current [1]		I_S	-	-	16.2	A	
Pulsed Source Current [2 3]		I_{SM}	-	-	60		
Forward on Voltage [3]		V_{SD}	-	-	1.2	V	I_S=1A, V_{GS}=0
Reverse Recovery Time		T_{rr}	-	15	-	nS	I_F=15A, dI/dt=100A/μs, T_J=25°C
Reverse Recovery Charge		Q_{rr}	-	25	-	nC	

Notes:
1. The data tested by Surface mounted on a 1 inch^2 FR-4 board with 2oz copper.
2. The power dissipation is limited by 150°C junction temperature.
3. The data tested by pulsed, pulse width≤300μs, duty cycle≤2%.

CHARACTERISTIC CURVES

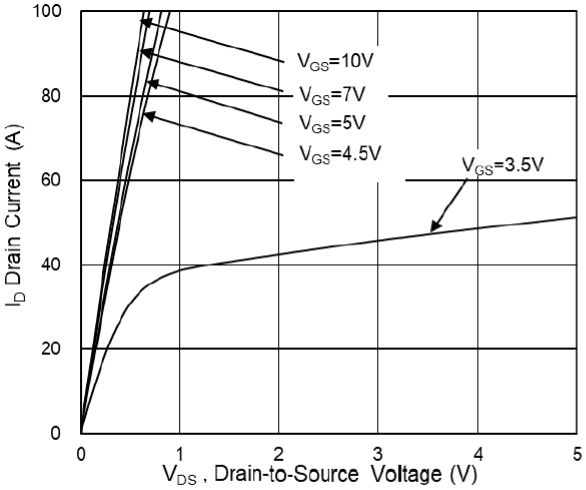


Fig.1 Typical Output Characteristics

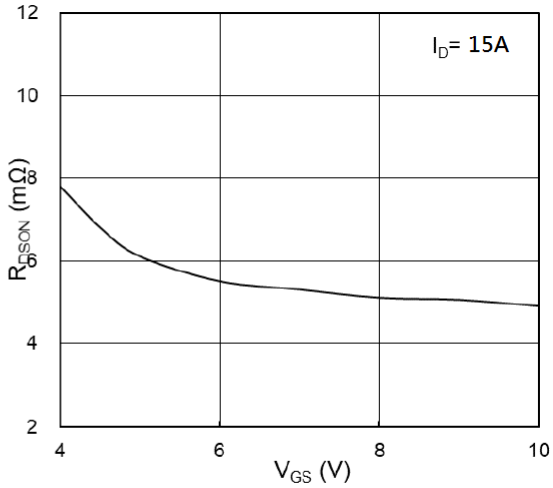


Fig.2 On-Resistance vs G-S Voltage

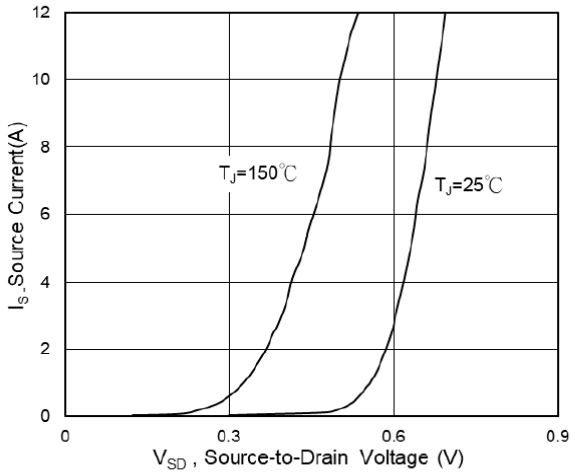


Fig.3 Source Drain Forward Characteristics

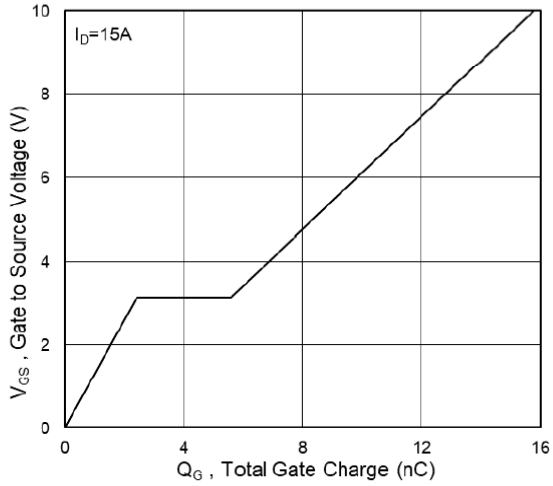


Fig.4 Gate-Charge Characteristics

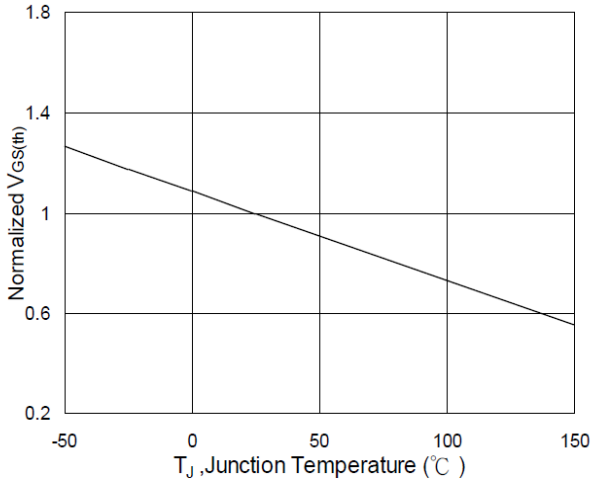


Fig.5 Normalized $V_{GS(th)}$ vs T_J

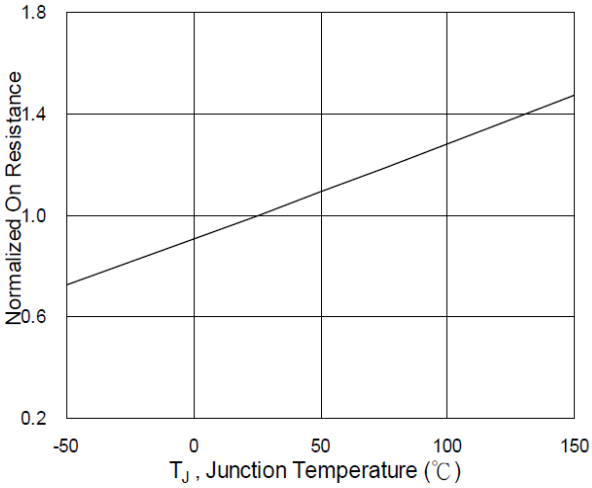


Fig.6 Normalized R_{DSON} vs T_J

CHARACTERISTIC CURVES

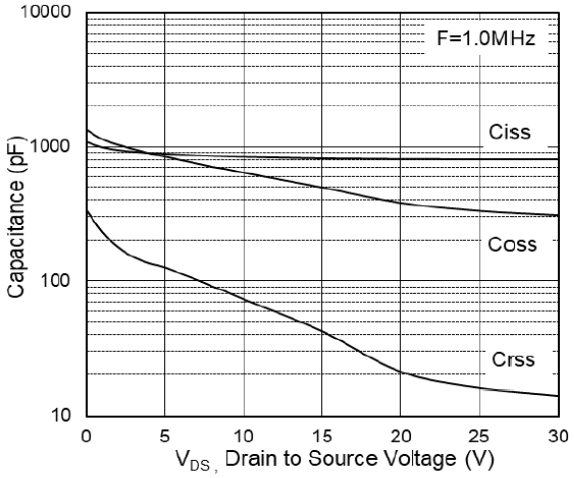


Fig.7 Capacitance

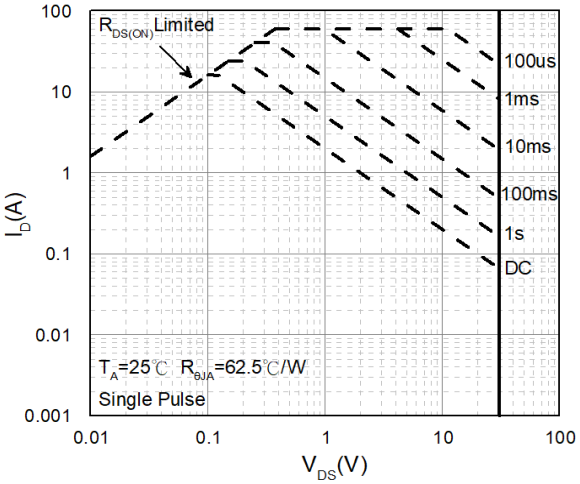


Fig.8 Safe Operating Area

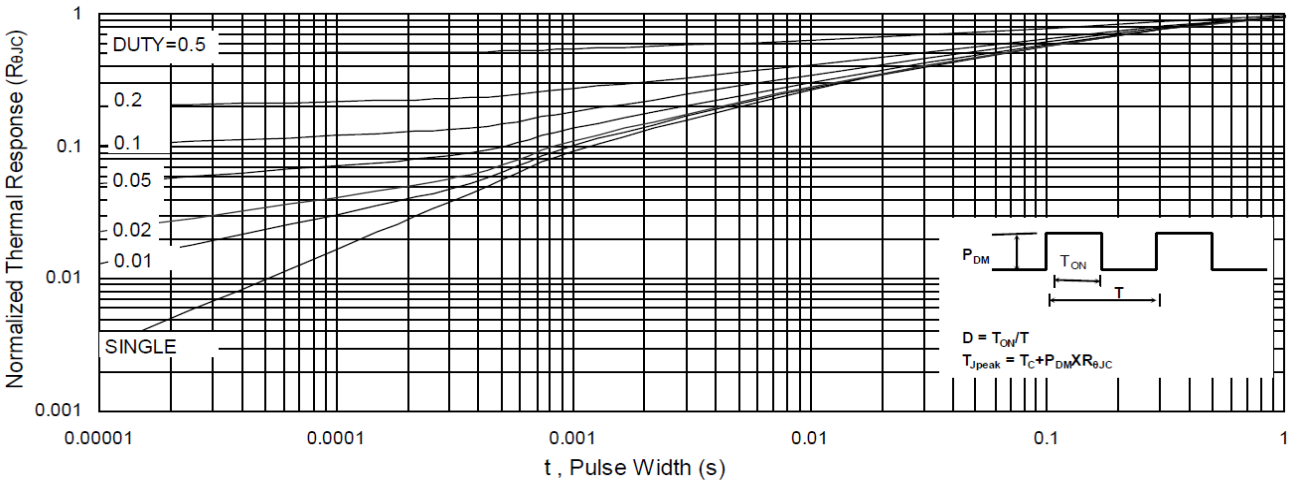


Fig.9 Normalized Maximum Transient Thermal Impedance

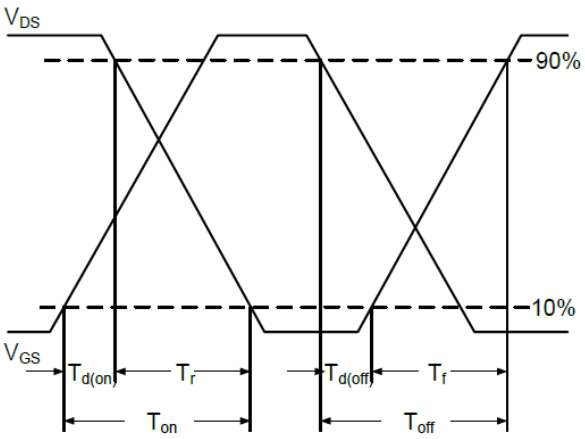


Fig.10 Switching Time Waveform

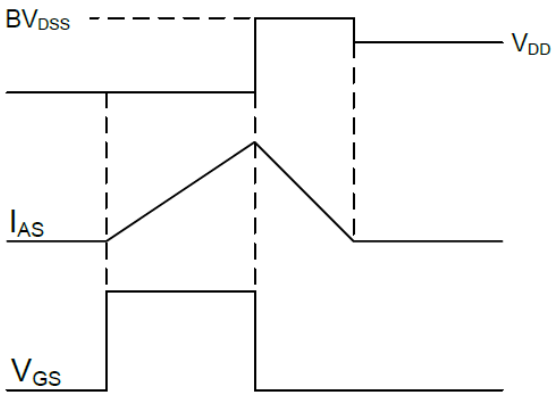


Fig.11 Unclamped Inductive Waveform