Elektronische Bauelemente

SSG4504

N & P-Ch Enhancement Mode Power MOSFET

N-Ch: 7.2 A, 40 V, $R_{DS(ON)}$ 30 mΩ

P-Ch: -6.5A, -40 V, $R_{DS(ON)}$ 40 mΩ

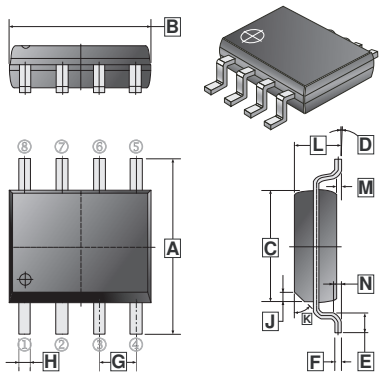
RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

The SSG4504 is the highest performance trench N-ch and P-ch MOSFETs with extreme high cell density, which provide excellent R_{DSON} and gate charge for most of the synchronous buck converter applications.

The SSG4504 meet the RoHS and Green Product requirement with full function reliability approved.

SOP-8

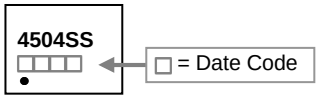


REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.79	6.20	H	0.33	0.51
B	4.70	5.11	J	0.375 REF.	
C	3.80	4.00	K	45°REF.	
D	0°	8°	L	1.3	1.752
E	0.40	1.27	M	0	0.25
F	0.10	0.25	N	0.25 REF.	
G	1.27 TYP.				

FEATURES

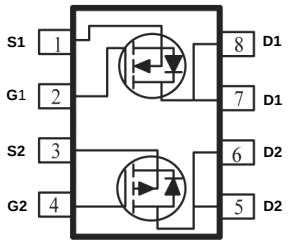
- Advanced high cell density Trench technology
- Super Low Gate Charge
- Green Device Available

MARKING



PACKAGE INFORMATION

Package	MPQ	Leader Size
SOP-8	2.5K	13 inch



ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Ratings		Unit
			N-Ch	P-Ch	
Drain-Source Voltage		V_{DS}	40	-40	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current [1], V_{GS}@10V	T_A=25℃	I_D	7.2	-6.5	A
	T_A=100℃		5.6	-5.1	A
Pulsed Drain Current [3]		I_{DM}	14.5	-13	A
Total Power Dissipation	T_C=25℃	P_D	2.5		W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150		℃
Thermal Data					
Thermal Resistance Junction-ambient [1]		$R_{\theta JA}$	85		℃ / W
Thermal Resistance Junction-ambient [2]		$R_{\theta JA}$	135		
Thermal Resistance Junction-case [1]		$R_{\theta JC}$	50		

N-CHANNEL ELECTRICAL CHARACTERISTICS (T_J=25℃ unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		BV_{DSS}	40	-	-	V	V_{GS}=0, I_D=250uA
Gate Threshold Voltage		$V_{GS(th)}$	1.0	-	2.5	V	V_{DS}=V_{GS}, I_D=250uA
Forward Transfer conductance		g_{fs}	-	14	-	S	V_{DS}=5V, I_D=6A
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS} = ±20V
Drain-Source Leakage Current	T_J=25℃	I_{DSS}	-	-	1	uA	V_{DS}=32V, V_{GS}=0
	T_J=55℃		-	-	5		
Static Drain-Source On-Resistance [4]		$R_{DS(ON)}$	-	-	30	mΩ	V_{GS}=10V, I_D=6A
			-	-	40		V_{GS}=4.5V, I_D=4A
Total Gate Charge		Q_g	-	5.5	-	nC	I_D=6A V_{DS}=20V V_{GS}=4.5V
Gate-Source Charge		Q_{gs}	-	1.25	-		
Gate-Drain (“Miller”) Change		Q_{gd}	-	2.5	-		
Turn-on Delay Time		$T_{d(on)}$	-	8.9	-	nS	V_{DD}=20V V_{GS}=10V I_D=1A R_G=3.3Ω R_D=20Ω
Rise Time		T_r	-	2.2	-		
Turn-off Delay Time		$T_{d(off)}$	-	41	-		
Fall Time		T_f	-	2.7	-		
Input Capacitance		C_{iss}	-	593	-	pF	V_{GS}=0 V_{DS}=15V f=1.0MHz
Output Capacitance		C_{oss}	-	76	-		
Reverse Transfer Capacitance		C_{rss}	-	56	-		
Source-Drain Diode							
Forward On Voltage [4]		V_{SD}	-	-	1.2	V	I_S=1A, V_{GS}=0, T_J=25℃
Continuous Source Current [1]		I_S	-	-	7.2	A	
Pulsed Source Current [3]		I_{SM}	-	-	14.5	A	

Notes:
1. Surface mounted on a 1 inch^2 FR-4 board with 2OZ copper
2. When mounted on Min. copper pad.
3. Pulse width limited by maximum junction temperature , pulse width ≦ 300us , duty cycle ≦ 2%
4. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

P-CHANNEL ELECTRICAL CHARACTERISTICS (T_J=25℃ unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		BV_{DSS}	-40	-	-	V	V_{GS}=0, I_D= -250uA
Gate Threshold Voltage		$V_{GS(th)}$	-1	-	-2.5	V	V_{DS}=V_{GS}, I_D= -250uA
Forward Transfer conductance		g_{fs}	-	12	-	S	V_{DS}= -5V, I_D= -6A
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}=±20V
Drain-Source Leakage Current	T_J=25℃	I_{DSS}	-	-	-1	uA	V_{DS}= -32V, V_{GS}=0
	T_J=55℃		-	-	-5		
Static Drain-Source On-Resistance [4]		$R_{DS(ON)}$	-	-	40	mΩ	V_{GS}= -10V, I_D= -6A
			-	-	65		V_{GS}= -4.5V, I_D= -4A
Total Gate Charge		Q_g	-	9	-	nC	I_D= -6A V_{DS}= -20V V_{GS}= -4.5V
Gate-Source Charge		Q_{gs}	-	2.54	-		
Gate-Drain (“Miller”) Change		Q_{gd}	-	3.1	-		
Turn-on Delay Time		$T_{d(on)}$	-	19.2	-	nS	V_{DS}= -15V V_{GS}= -10V I_D= -1A R_G=3.3Ω R_D=20Ω
Rise Time		T_r	-	12.8	-		
Turn-off Delay Time		$T_{d(off)}$	-	48.6	-		
Fall Time		T_f	-	4.6	-		
Input Capacitance		C_{iss}	-	1004	-	pF	V_{GS}=0 V_{DS}= -15V f=1.0MHz
Output Capacitance		C_{oss}	-	108	-		
Reverse Transfer Capacitance		C_{rss}	-	80	-		
Source-Drain Diode							
Forward On Voltage [1]		V_{SD}	-	-	-1	V	I_S= -1A, V_{GS}=0V, T_J=25℃
Continuous Source Current [3]		I_S	-	-	-6.5	A	
Pulsed Source Current [4]		I_{SM}	-	-	-13	A	

Notes:
1. Surface mounted on a 1 inch^2 FR-4 board with 2OZ copper
2. When mounted on Min. copper pad.
3. Pulse width limited by maximum junction temperature , pulse width ≦ 300us , duty cycle ≦ 2%
4. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

CHARACTERISTIC CURVE (N-Ch)

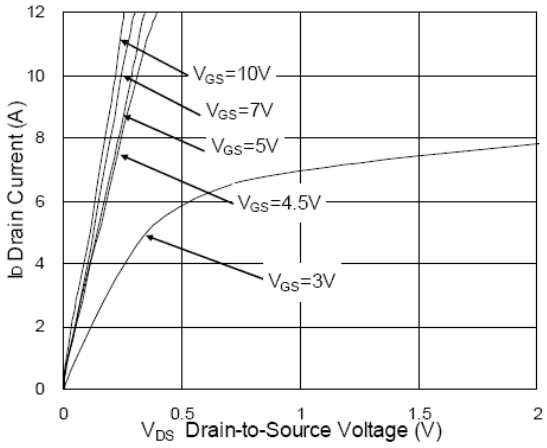


Fig.1 Typical Output Characteristics

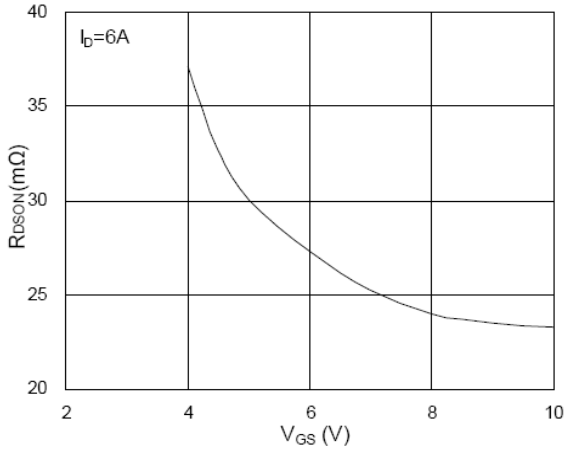


Fig.2 On-Resistance vs. G-S Voltage

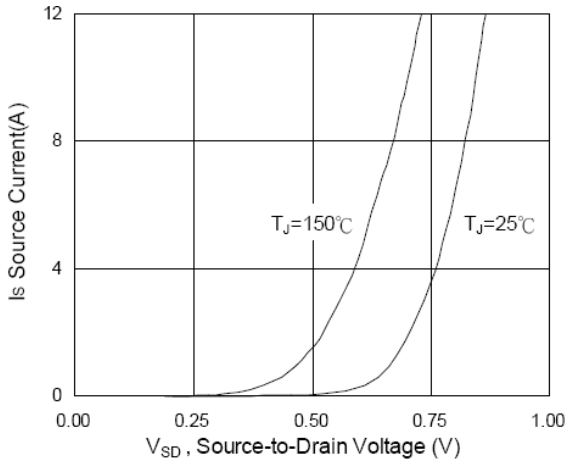


Fig.3 Forward Characteristics of Reverse

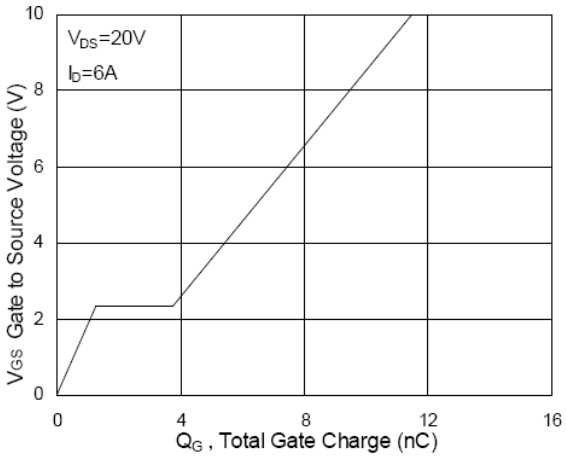


Fig.4 Gate-Charge Characteristics

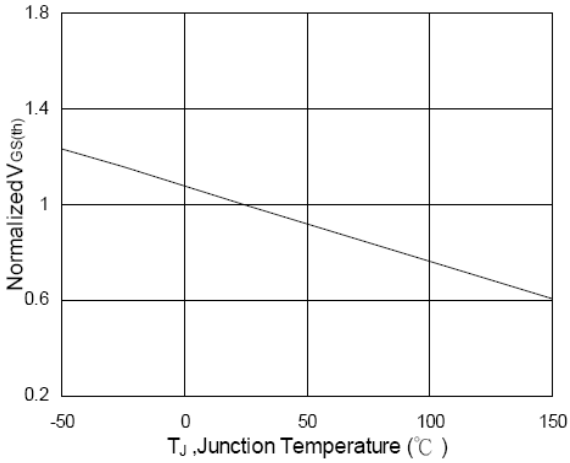


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

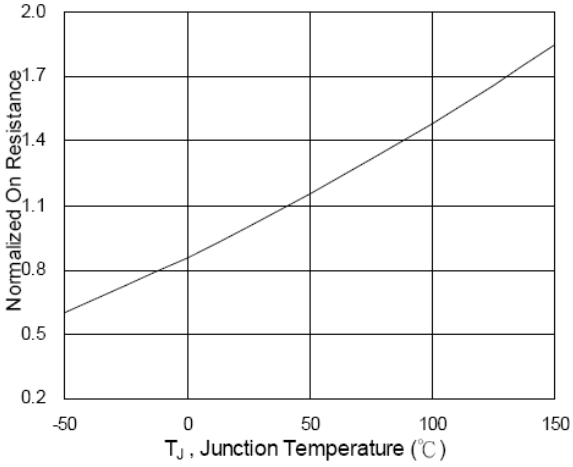


Fig.6 Normalized R_{DSON} vs. T_J

CHARACTERISTIC CURVE (N-Ch)

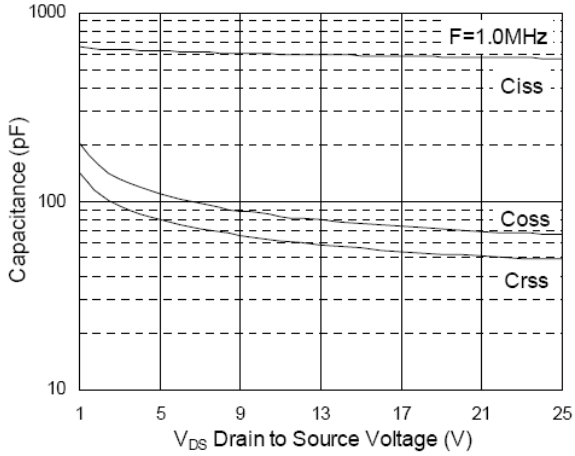


Fig.7 Capacitance

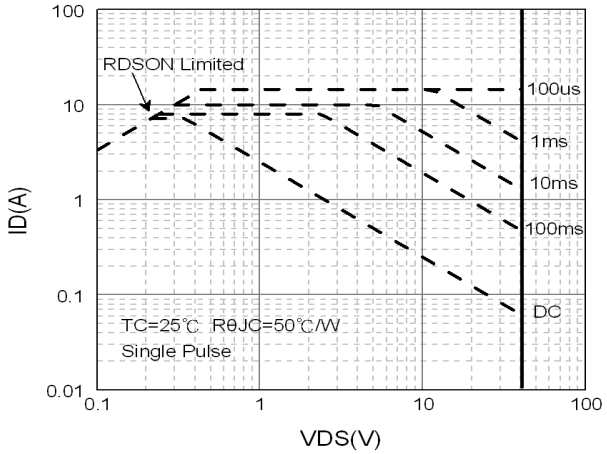


Fig.8 Safe Operating Area

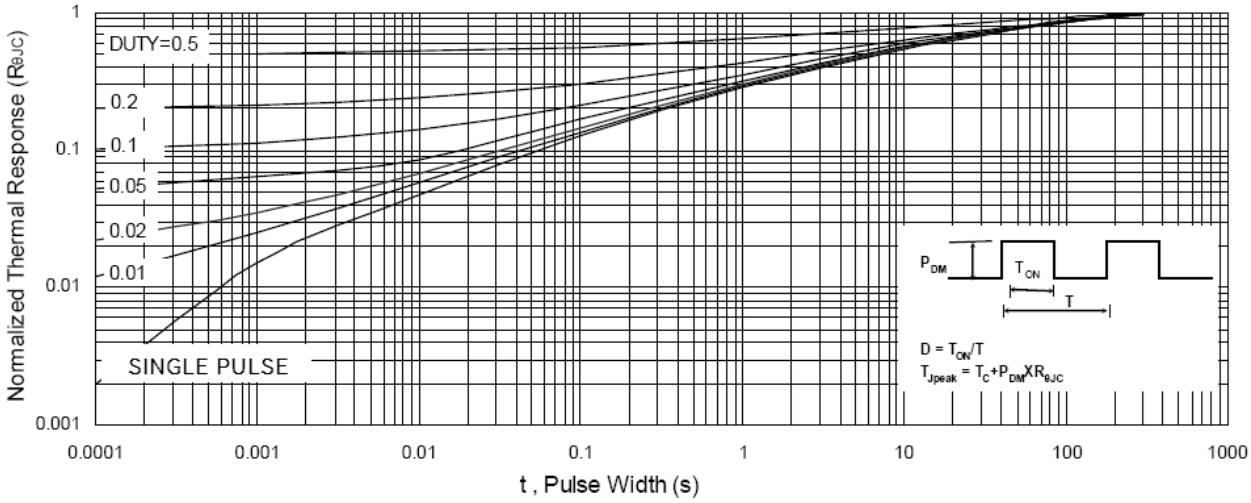


Fig.9 Normalized Maximum Transient Thermal Impedance

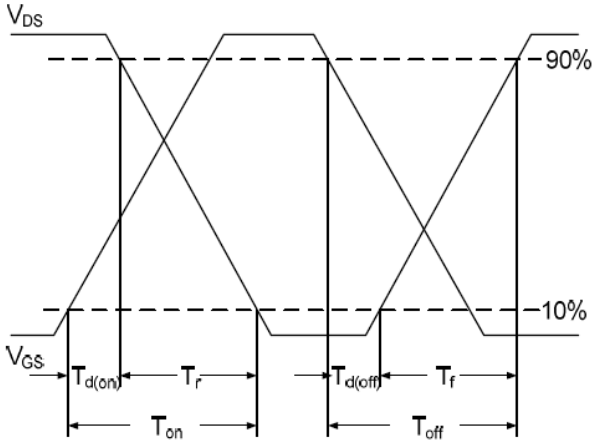


Fig.10 Switching Time Waveform

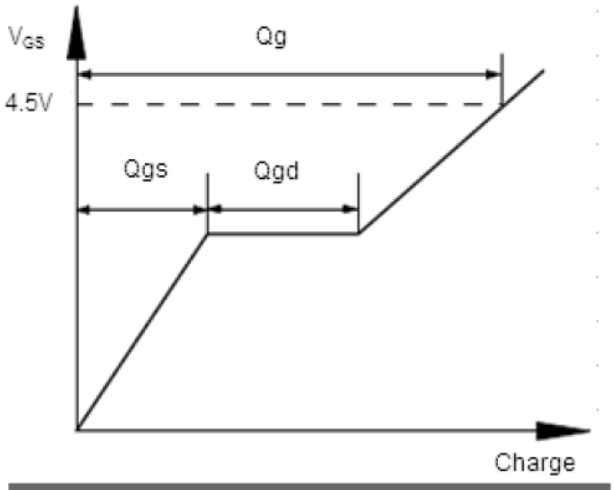


Fig.11 Gate Charge Waveform

CHARACTERISTIC CURVE (P-Ch)

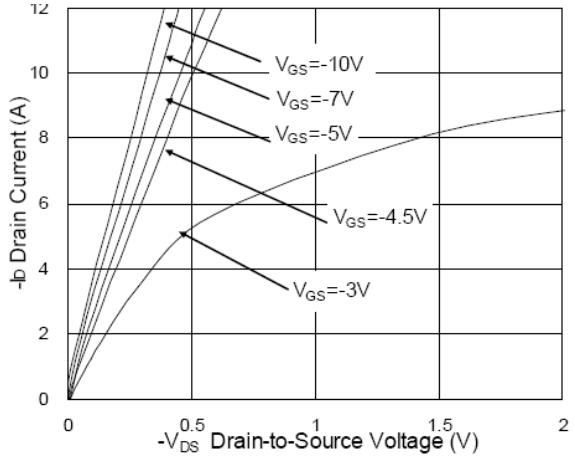


Fig.1 Typical Output Characteristics

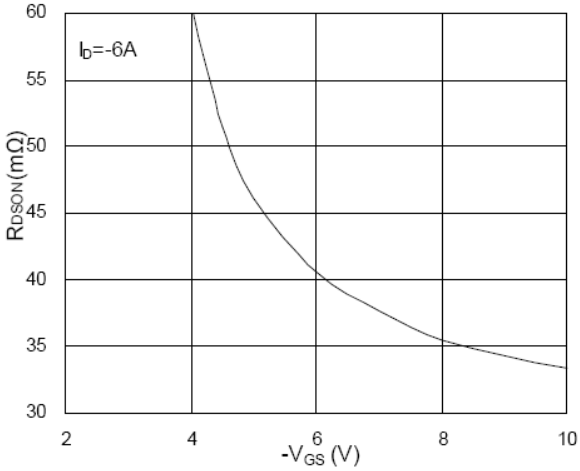
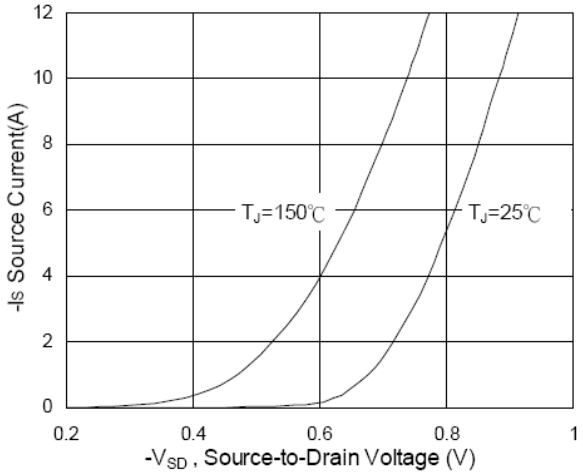


Fig.2 On-Resistance v.s Gate-Source



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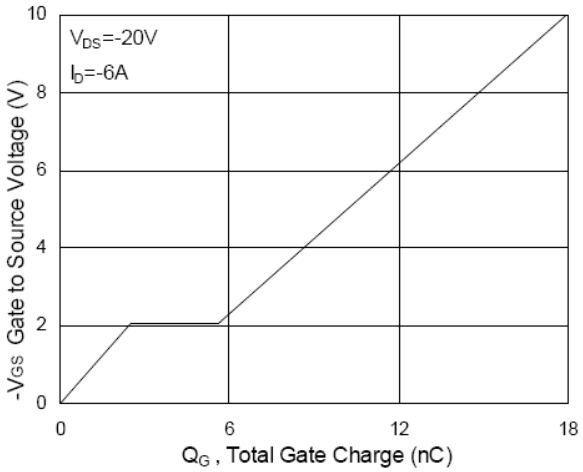


Fig.4 Gate-Charge Characteristics

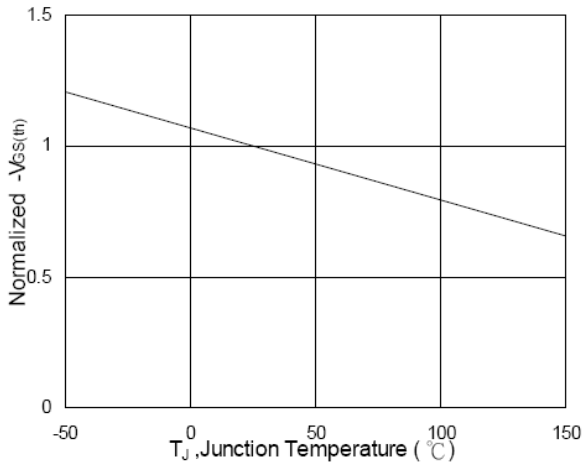


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

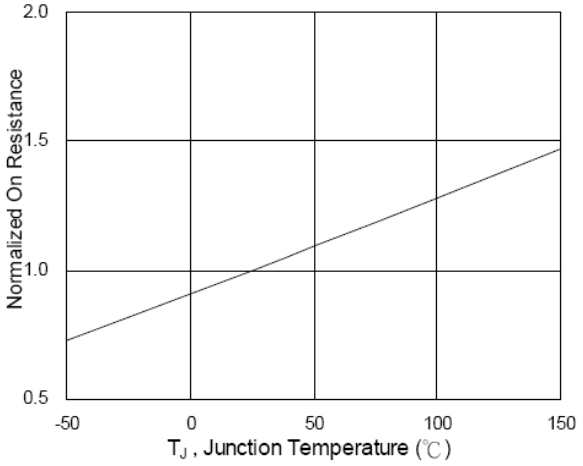


Fig.6 Normalized R_{DSON} v.s T_J

CHARACTERISTIC CURVE (P-Ch)

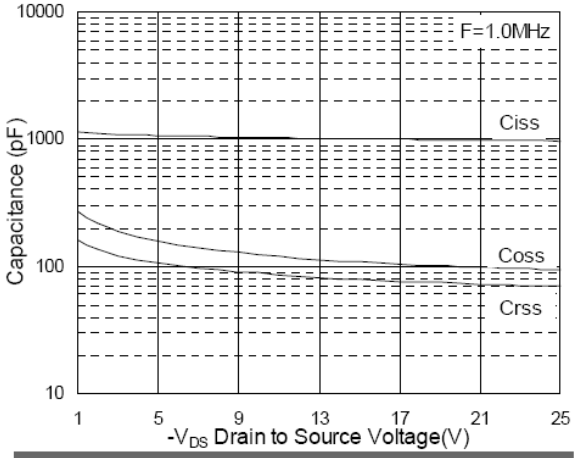
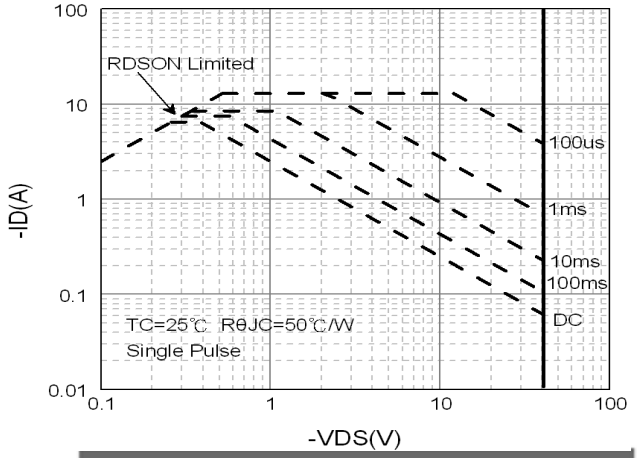


Fig.7 Capacitance



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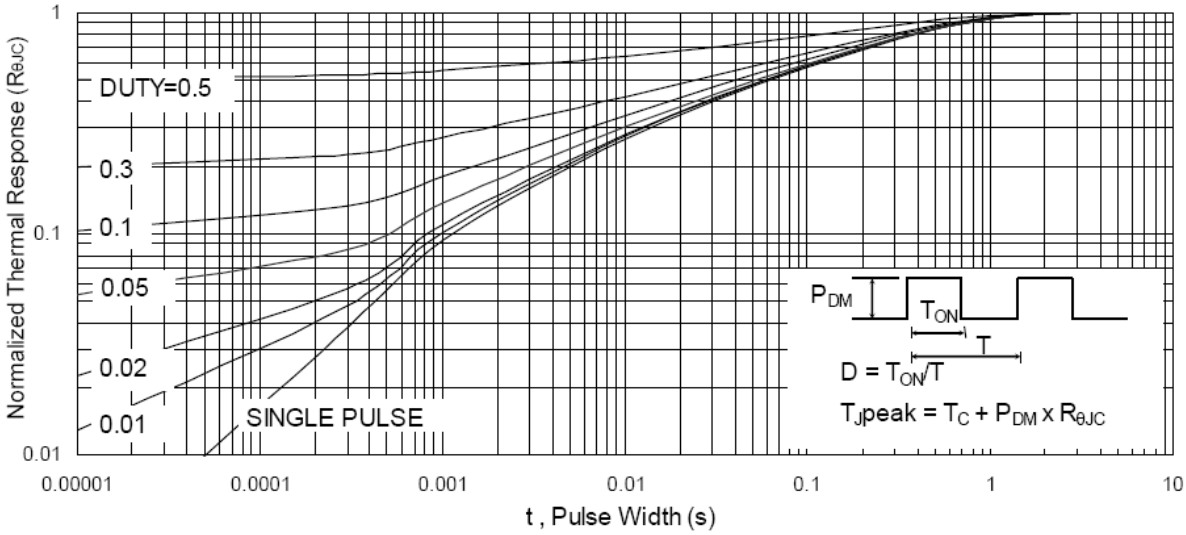

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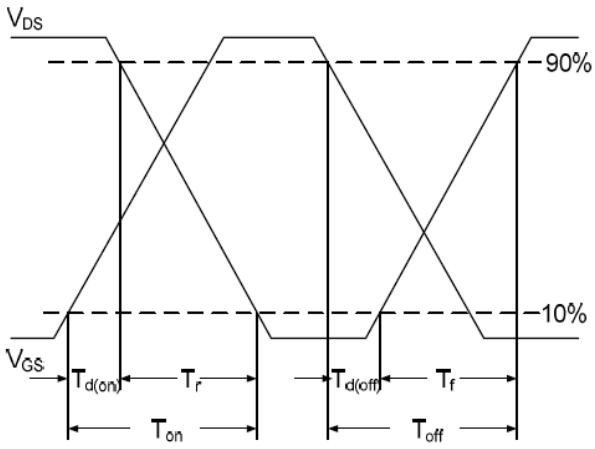

Fig.10 Switching Time Waveform

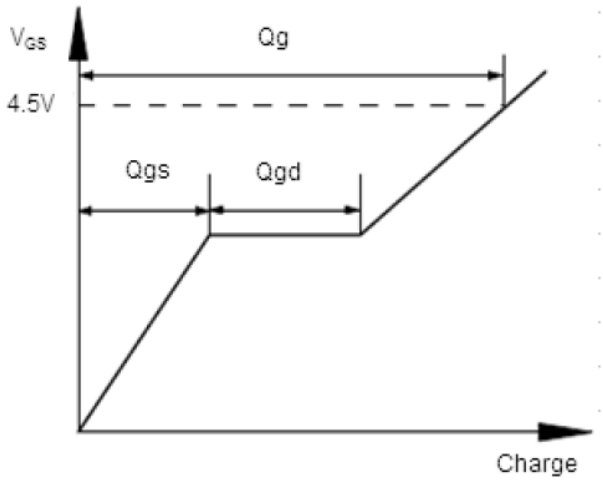

Fig.11 Gate Charge Waveform