Elektronische Bauelemente

SMS4101-C

-3.7A, -40V, $R_{DS(ON)}$ 70mΩ

P-Channel Enhancement Mode Power MOSFET

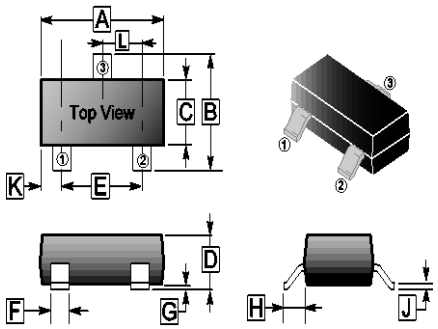
RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

The SMS4101-C is the highest performance trench P-ch MOSFETs with extreme high cell density, which provide Excellent $R_{DS(ON)}$ and gate charge for most of the small power switching and load switch applications.

The SMS4101-C meet the RoHS and Green Product requirement with full function reliability approved.

SOT-23



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.65	3.10	G	0	0.18
B	2.10	3.00	H	0.55 REF.	
C	1.10	1.80	J	0.05	0.26
D	0.89	1.40	K	0.60 REF.	
E	1.70	2.30	L	0.95 TYP.	
F	0.28	0.55			

FEATURES

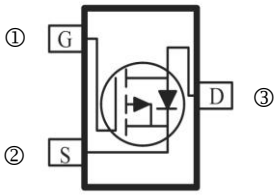
- Advanced High Cell Density Trench Technology
- Super low Gate Charge
- Green Device Available

PACKAGE INFORMATION

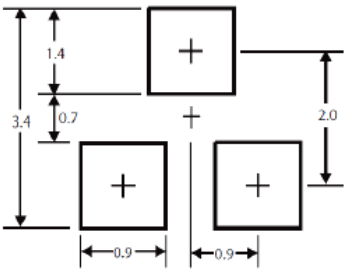
Package	MPQ	Leader Size
SOT-23	3K	7 inch

ORDER INFORMATION

Part Number	Type
SMS4101-C	Lead (Pb)-free and Halogen-free



Mounting Pad Layout



*Dimensions in millimeters

ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise specified)

Parameter		Symbol	Rating		Unit
			10sec	Steady State	
Drain-Source Voltage		V_{DS}	-40		V
Continuous Gate-Source Voltage		V_{GS}	±20		V
Continuous Drain Current [1] @V_{GS}= -10V	T_A=25°C	I_D	-3.7	-3.2	A
	T_A=70°C		-3	-2.6	
Pulsed Drain Current [2]		I_{DM}	-16		A
Total Power Dissipation [3]	T_A=25°C	P_D	1.32	1	W
	T_A=70°C		0.84	0.64	
Operating Junction & Storage Temperature Range		T_J, T_{STG}	150, -55~150		°C
Thermal Resistance Ratings					
Thermal Resistance from Junction-Ambient [1]		$R_{\theta JA}$	125		°C/W
Thermal Resistance from Junction-Ambient [1]	t ≤10s		95		
Thermal Resistance from Junction-Case [1]		$R_{\theta JC}$	80		

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		BV_{DSS}	-40	-	-	V	V_{GS}=0, I_D= -250μA
Gate-Source Threshold Voltage		$V_{GS(th)}$	-1	-	-2.5	V	V_{DS}=V_{GS}, I_D= -250μA
Forward Transconductance		g_{fs}	-	5.8	-	S	V_{DS}= -5V, I_D= -3A
Drain-Source Leakage Current	T_J=25°C	I_{DSS}	-	-	-1	μA	V_{GS}=0, V_{DS}= -24V
	T_J=55°C		-	-	-5		
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}=±20V, V_{DS}=0
Static Drain-Source On Resistance [2]		$R_{DS(ON)}$	-	-	70	mΩ	V_{GS}= -10V, I_D= -3A
			-	-	100		V_{GS}= -4.5V, I_D= -2A
Total Gate Charge		Q_g	-	6.4	-	nC	V_{DS}= -32V V_{GS}= -4.5V I_D= -3A
Gate-Source Charge		Q_{gs}	-	2.1	-		
Gate-Drain (“Miller”) Charge		Q_{gd}	-	2.5	-		
Turn-On Delay Time		$T_{d(on)}$	-	4.2	-	nS	I_D= -3A V_{DD}= -20V V_{GS}= -4.5V R_G=3.3Ω
Rise Time		T_r	-	23	-		
Turn-Off Delay Time		$T_{d(off)}$	-	26.8	-		
Fall Time		T_f	-	20.6	-		
Input Capacitance		C_{iss}	-	620	-	pF	V_{DS}= -15V V_{GS}=0 f=1MHz
Output Capacitance		C_{oss}	-	65	-		
Reverse Transfer Capacitance		C_{rss}	-	53	-		
Source Drain Diode							
Continuous Source Current [1 4]		I_S	-	-	-3.2	A	V_G=V_D=0V, Force Current
Pulsed Source Current [2 4]		I_{SM}	-	-	-16		
Forward On Voltage [2]		V_{SD}	-	-	-1	V	V_{GS}=0, I_S= -1A, T_J=25°C

Notes:
1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2oz copper.
2. The data tested by pulsed, pulse width≦300us, duty cycle≦2%.
3. The power dissipation is limited by 150°C junction temperature.
4. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

TYPICAL CHARACTERISTIC CURVE

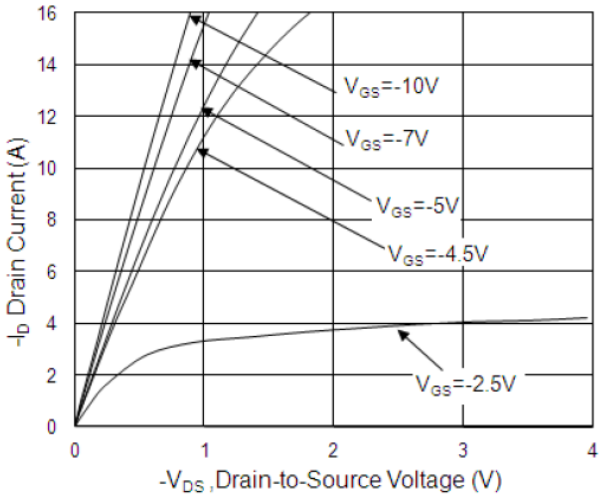


Fig.1 Typical Output Characteristics

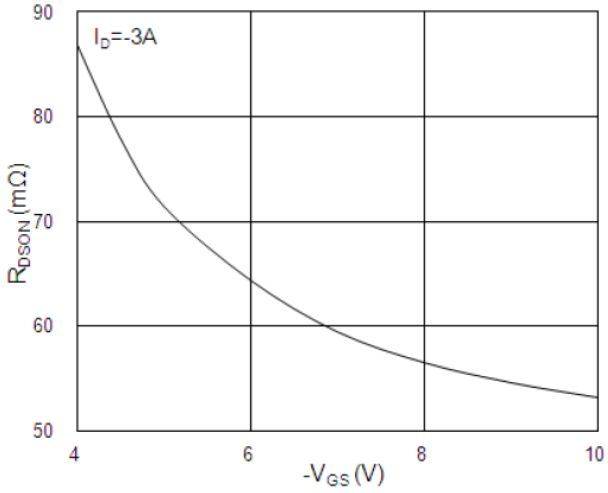


Fig.2 On-Resistance vs. G-S Voltage

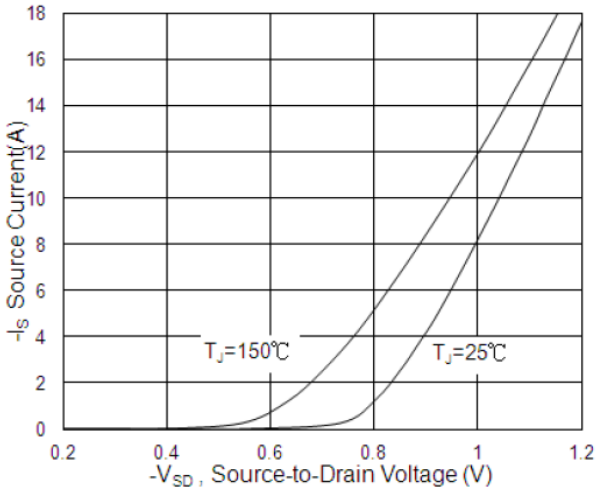


Fig.3 Forward Characteristics Of Reverse

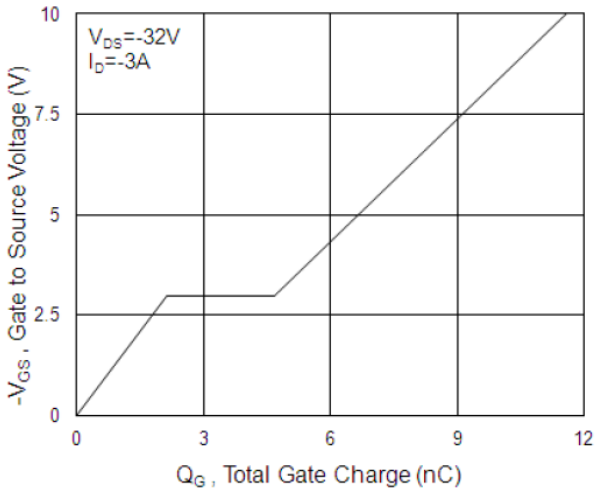


Fig.4 Gate-Charge Characteristics

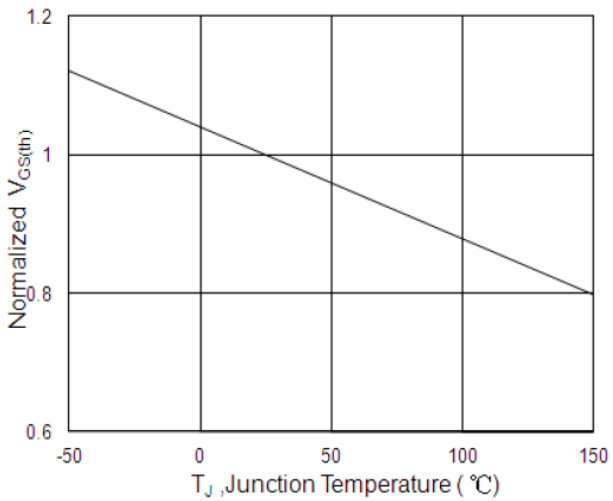


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

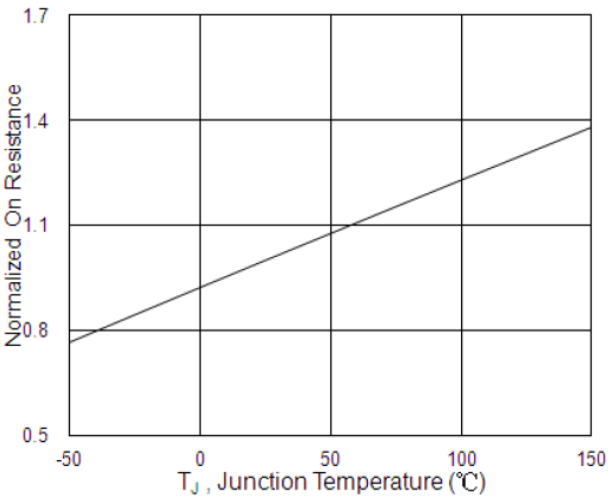


Fig.6 Normalized R_{DSON} vs. T_J

TYPICAL CHARACTERISTIC CURVE

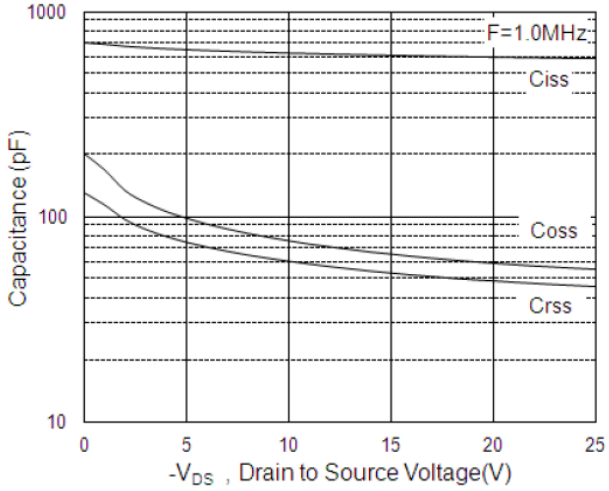


Fig.7 Capacitance

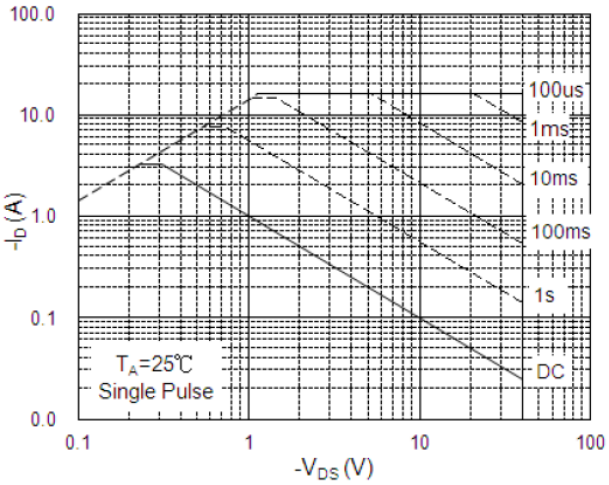


Fig.8 Safe Operating Area

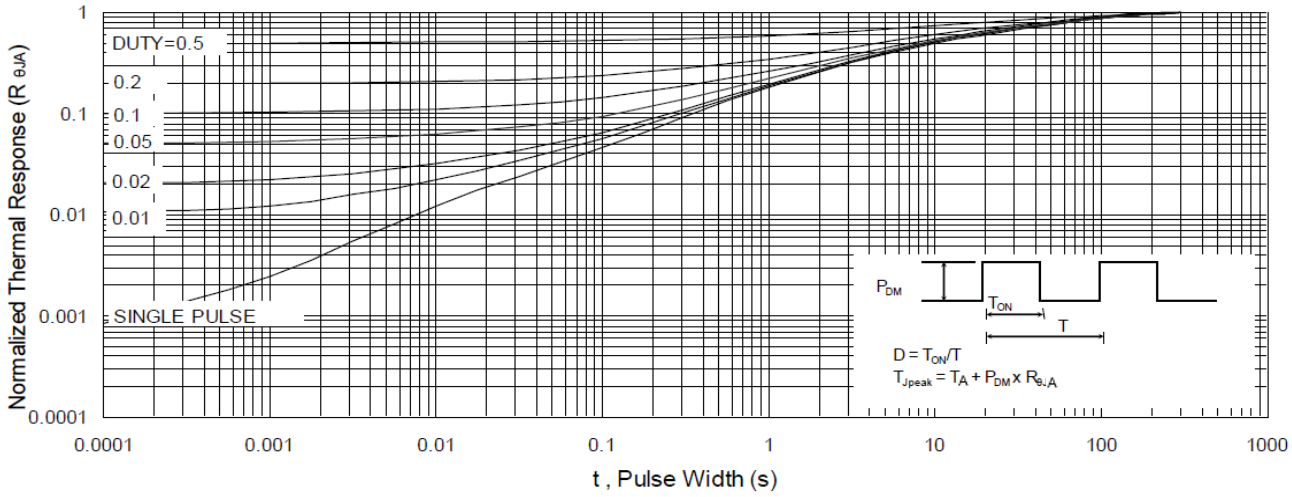


Fig.9 Normalized Maximum Transient Thermal Impedance

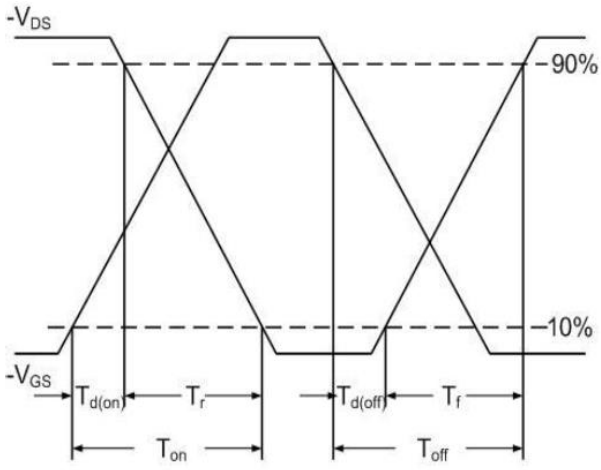


Fig.10 Switching Time Waveform

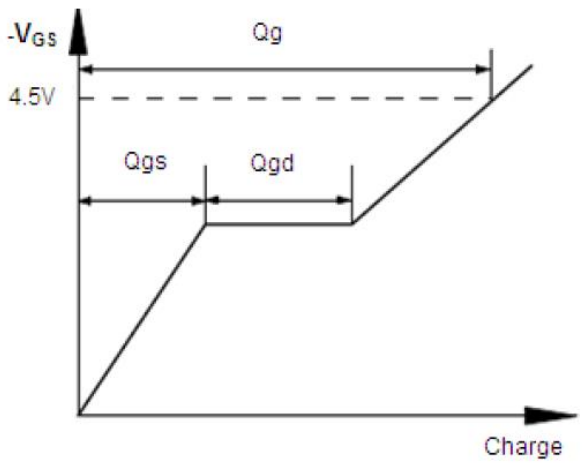


Fig.11 Gate Charge Waveform