

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

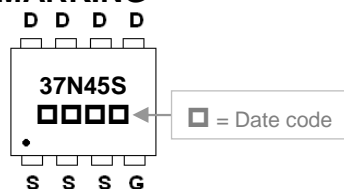
The SSPR37N45S-C is the highest performance trench N-Ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The SSPR37N45S-C meet the RoHS and Green Product requirement with full function reliability approved.

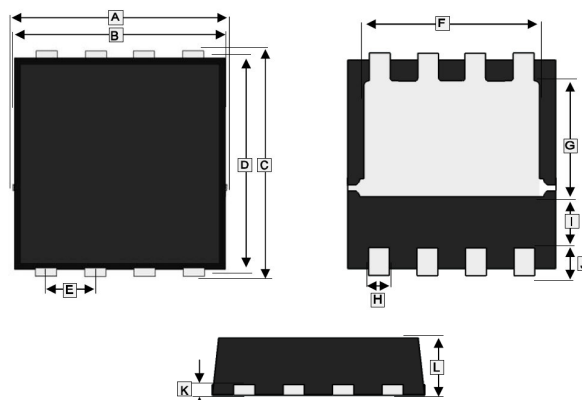
FEATURES

- Advanced High Cell Density Trench Technology
- Super Low Gate Charge
- Green Device Available

MARKING



SPR-8PP



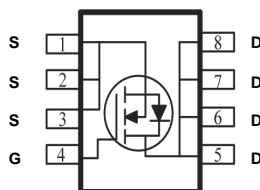
REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	3.00	3.40	G	1.35	1.98
B	3.00	3.25	H	0.24	0.35
C	3.20	3.45	I	0.35 TYP.	
D	3.00	3.20	J	0.60 TYP.	
E	0.65 BSC.		K	0.10	0.25
F	2.39	2.60	L	0.70	0.90

PACKAGE INFORMATION

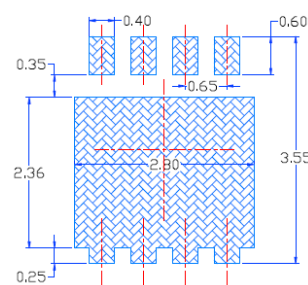
Package	MPQ	Leader Size
SPR-8PP	3K	13 inch

ORDER INFORMATION

Part Number	Type
SSPR37N45S-C	Lead (Pb)-free and Halogen-free



Mounting Pad Layout



*Dimensions in millimeters

ABSOLUTE MAXIMUM RATINGS $T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	45	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ¹ (Silicon Limited)	I_D	$T_C=25^\circ\text{C}$	37
		$T_C=100^\circ\text{C}$	23
Continuous Drain Current ¹ (Package Limited)	I_D	26	A
Pulsed Drain Current ^{2,4}	I_{DM}	100	A
Power Dissipation	P_D	25	W
Operating Junction & Storage Temperature	T_J, T_{STG}	-55~150	$^\circ\text{C}$
Thermal Resistance Ratings			
Thermal Resistance Junction-Ambient ¹	$R_{\theta JA}$	55	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-Case ¹	$R_{\theta JC}$	5	

ELECTRICAL CHARACTERISTICS ($T_J=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Drain-Source Breakdown Voltage	BV_{DSS}	45	-	-	V	$V_{GS}=0, I_D=250\mu\text{A}$	
Gate-Threshold Voltage	$V_{GS(th)}$	1	-	2.2	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	
Gate-Source Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 20\text{V}$	
Drain-Source Leakage Current	I_{DSS}	$T_J=25^\circ\text{C}$	-	-	1	uA	$V_{DS}=36\text{V}, V_{GS}=0$
		$T_J=100^\circ\text{C}$	-	-	100		$V_{DS}=36\text{V}, V_{GS}=0$
Static Drain-Source On-Resistance ³	$R_{DS(ON)}$	-	7	9.5	m Ω	$V_{GS}=10\text{V}, I_D=10\text{A}$	
		-	9.6	14		$V_{GS}=4.5\text{V}, I_D=8\text{A}$	
Transconductance	g_{fs}	-	25	-	S	$V_{DS}=5\text{V}, I_D=15\text{A}$	
Gate Resistance	R_g	-	1.5	-	Ω	$V_{DS}=V_{GS}=0, f=1\text{MHz}$	
Total Gate Charge (4.5V)	Q_g	-	7	-	nC	$I_D=10\text{A}$ $V_{DD}=20\text{V}$ $V_{GS}=10\text{V}$	
Total Gate Charge		-	14.5	-			
Gate-Source Charge		-	2	-			
Gate-Drain Change		-	2.5	-			
Turn-on Delay Time	$T_{d(on)}$	-	6	-	nS	$V_{DD}=20\text{V}$ $I_D=10\text{A}$ $V_{GS}=10\text{V}$ $R_G=10\Omega$	
Rise Time	T_r	-	5	-			
Turn-off Delay Time	$T_{d(off)}$	-	21	-			
Fall Time	T_f	-	5	-			
Input Capacitance	C_{iss}	-	942	-	pF	$V_{GS}=0$ $V_{DS}=20\text{V}$ $f=1\text{MHz}$	
Output Capacitance	C_{oss}	-	309	-			
Reverse Transfer Capacitance	C_{rss}	-	29	-			
Source-Drain Diode							
Diode Forward Voltage ³	V_{SD}	-	-	1.2	V	$I_S=10\text{A}, V_{GS}=0$	
Reverse Recovery Time	T_{rr}	-	24	-	nS	$I_F=10\text{A}, V_R=20\text{V},$ $dI/dt=200\text{A}/\mu\text{s}$	
Reverse Recovery Charge	Q_{rr}	-	19	-	nC		

Notes:

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2oz copper.
2. The Pulse width limited by maximum junction temperature, Pulse Width $\leq 10\mu\text{s}$, Duty Cycle $\leq 2\%$.
3. The Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Package limit.

CHARACTERISTIC CURVES

Fig 1. Typical Output Characteristics

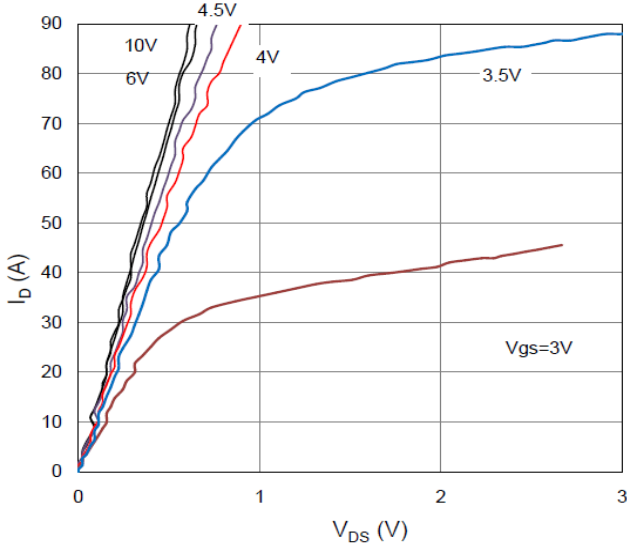


Figure 2. On-Resistance vs. Gate-Source Voltage

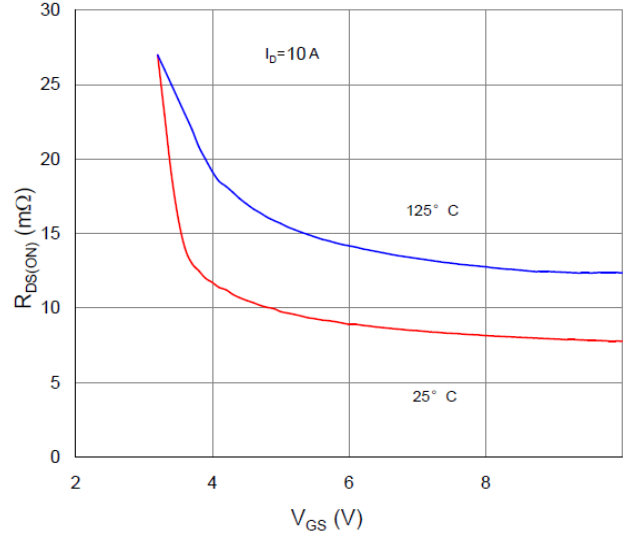


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

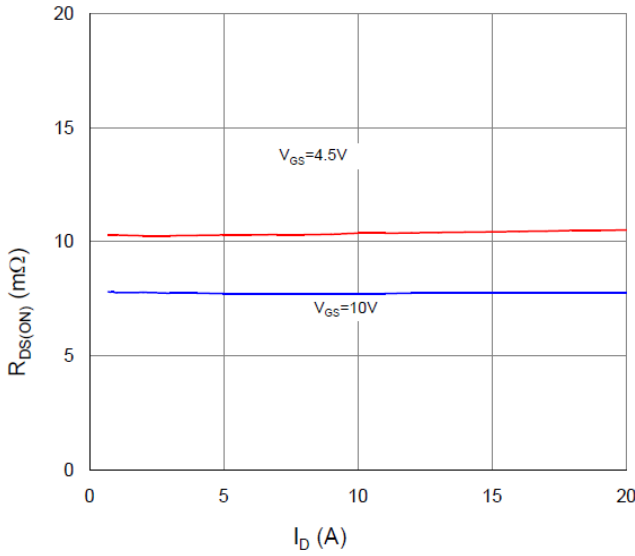


Figure 4. Normalized On-Resistance vs. Junction Temperature

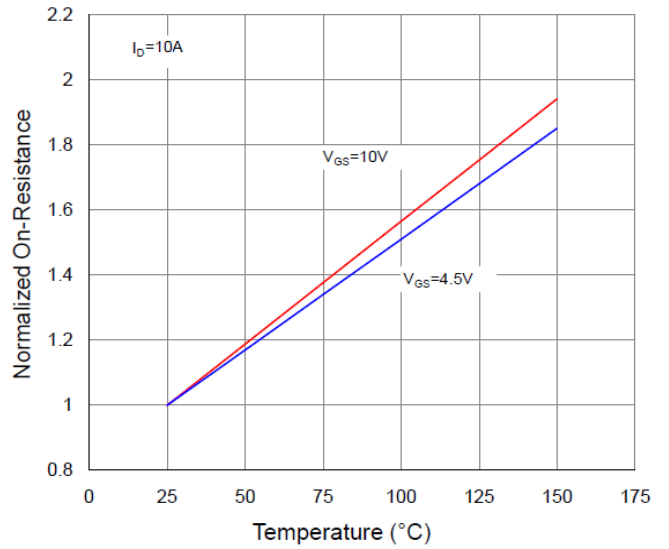


Figure 5. Typical Transfer Characteristics

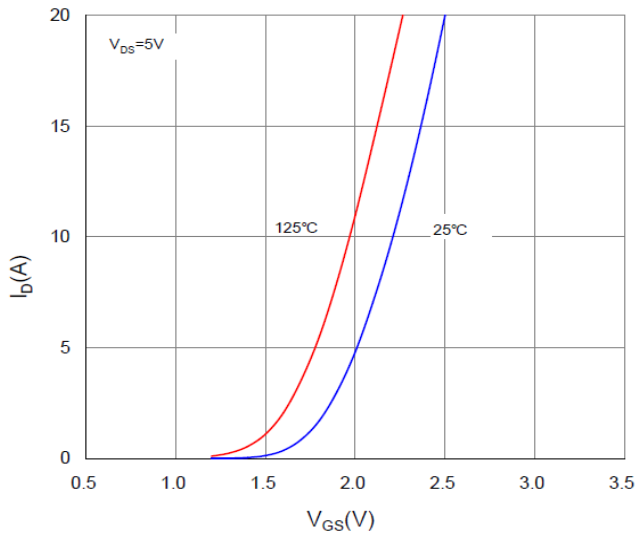
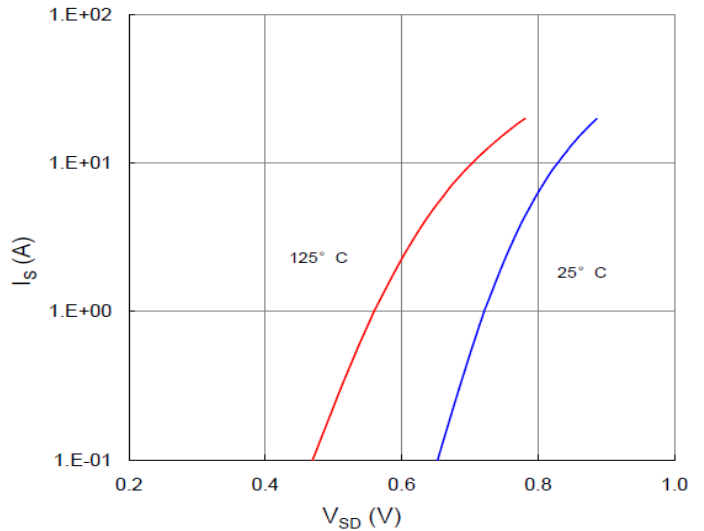


Figure 6. Typical Source-Drain Diode Forward Voltage



CHARACTERISTIC CURVES

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

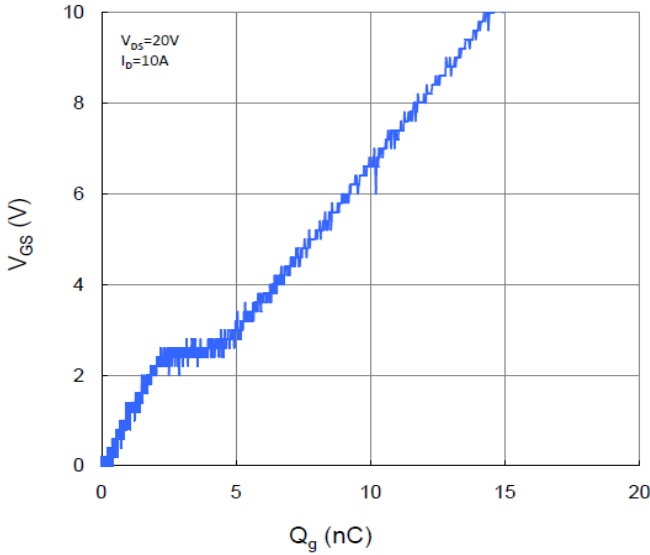


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

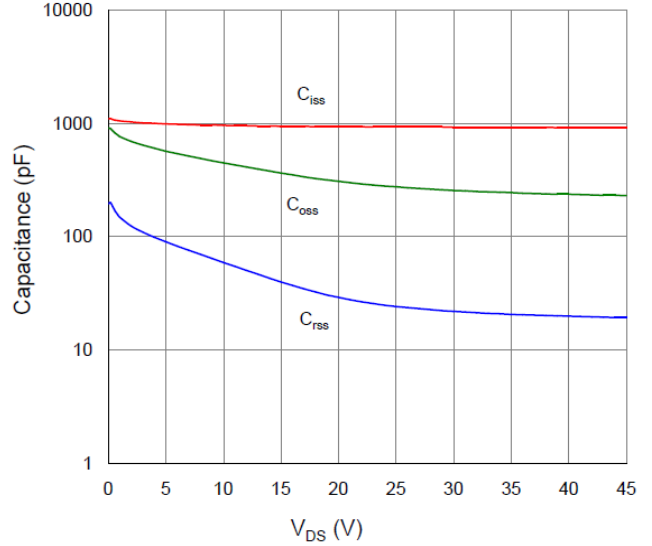


Figure 9. Maximum Safe Operating Area

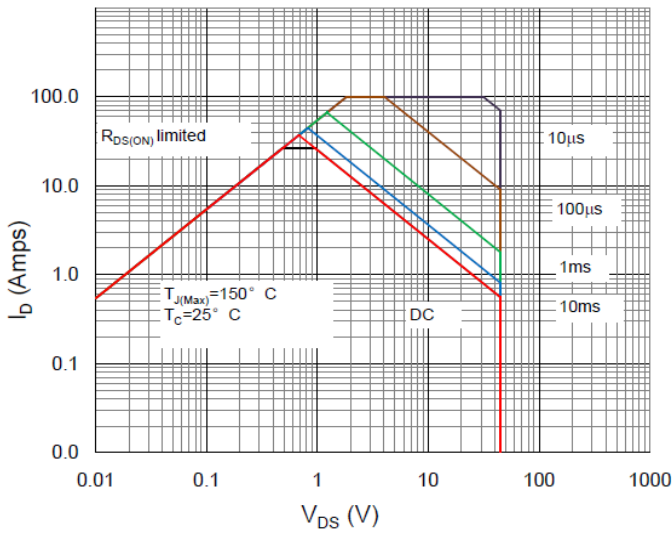


Figure 10. Maximum Drain Current vs. Case Temperature

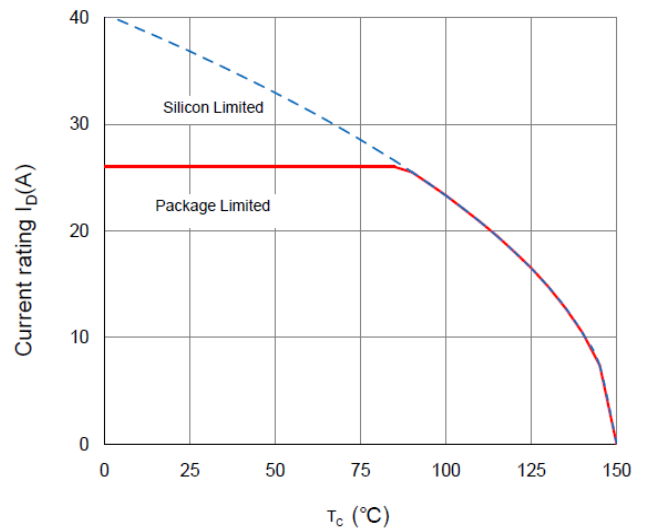


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case

