

RoHS Compliant Product  
A suffix of "-C" specifies halogen free

## DESCRIPTION

The SSE150N06SV-C is the Shielded Gate Technology N-ch MOSFETs with extreme high cell density, which provide excellent  $R_{DS(ON)}$  and gate charge for most of the synchronous buck converter applications.

The SSE150N06SV-C meet the RoHS and Green Product requirement with full function reliability approved.

## FEATURES

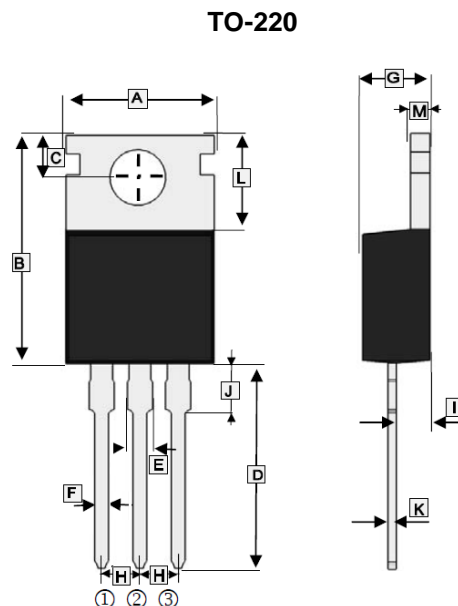
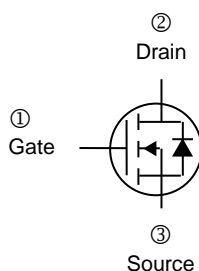
- Shielded Gate Trench Technology
- Super Low Gate Charge
- Green Device Available

## MARKING



## ORDER INFORMATION

Part Number	Type
SSE150N06SV-C	Lead (Pb)-free and Halogen-free



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	9.70	10.60	H	2.54 TYP.	
B	14.22	16.50	I	2.03	2.92
C	2.54	3.40	J	2.70	4.00
D	12.70	14.70	K	0.33	0.65
E	1.17	1.78	L	5.50	7.00
F	0.40	1.00	M	1.15	1.40
G	3.60	4.82			

## ABSOLUTE MAXIMUM RATINGS ( $T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>1</sup> @ $V_{GS}=10\text{V}$	$I_D$	$T_C=25^\circ\text{C}$	150
		$T_C=100^\circ\text{C}$	95
Pulsed Drain Current <sup>2</sup>	$I_{DM}$	300	A
Single Pulse Avalanche Energy <sup>4</sup>	$E_{AS}$	101	mJ
Single Pulse Avalanche Current	$I_{AS}$	45	A
Power Dissipation <sup>3</sup>	$P_D$	156	W
Operating Junction & Storage Temperature Range	$T_J, T_{STG}$	-55~150	$^\circ\text{C}$
Thermal Resistance Ratings			
Thermal Resistance Junction-Ambient <sup>1</sup>	$R_{\theta JA}$	62	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-Case <sup>1</sup>	$R_{\theta JC}$	0.8	

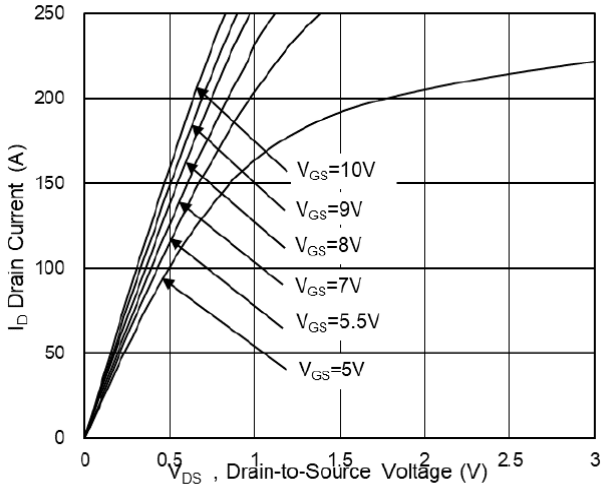
**ELECTRICAL CHARACTERISTICS** ( $T_J=25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0V, I_D=250\mu A$	
Gate Threshold Voltage	$V_{GS(th)}$	2	-	4	V	$V_{DS}=V_{GS}, I_D=250\mu A$	
Forward Transconductance	$g_{fs}$	-	65	-	S	$V_{DS}=5V, I_D=20A$	
Gate-Source Leakage Current	$I_{GSS}$	-	-	$\pm 100$	nA	$V_{GS}=\pm 20V$	
Drain-Source Leakage Current	$I_{DSS}$	$T_J=25^\circ\text{C}$	-	-	1	$\mu A$	$V_{DS}=48V, V_{GS}=0V$
		$T_J=55^\circ\text{C}$	-	-	5		$V_{DS}=48V, V_{GS}=0V$
Static Drain-Source On-Resistance <sup>2</sup>	$R_{DS(ON)}$	-	3.4	4.2	m $\Omega$	$V_{GS}=10V, I_D=20A$	
		-	4.9	6.2		$V_{GS}=7V, I_D=15A$	
Total Gate Charge	$Q_g$	-	59	-	nC	$I_D=20A$ $V_{DS}=30V$ $V_{GS}=10V$	
Gate-Source Charge	$Q_{gs}$	-	15	-			
Gate-Drain Charge	$Q_{gd}$	-	10	-			
Turn-on Delay Time	$T_{d(on)}$	-	20	-	nS	$V_{DD}=30V$ $I_D=20A$ $V_{GS}=10V$ $R_G=3\Omega$	
Rise Time	$T_r$	-	9	-			
Turn-off Delay Time	$T_{d(off)}$	-	60	-			
Fall Time	$T_f$	-	15	-			
Input Capacitance	$C_{iss}$	-	3509	-	pF	$V_{GS}=0V$ $V_{DS}=30V$ $f=1\text{MHz}$	
Output Capacitance	$C_{oss}$	-	1175	-			
Reverse Transfer Capacitance	$C_{rss}$	-	68	-			
<b>Source-Drain Diode</b>							
Diode Forward Voltage <sup>2</sup>	$V_{SD}$	-	-	1.2	V	$I_S=1A, V_{GS}=0V$	
Continuous Source Current <sup>1</sup>	$I_S$	-	-	150	A	$V_{DS}=V_{GS}=0V, \text{Force Current}$	
Reverse Recovery Time	$t_{rr}$	-	24	-	nS	$I_F=20A, di/dt=100A/\mu s,$ $T_J=25^\circ\text{C}$	
Reverse Recovery Charge	$Q_{rr}$	-	85	-	nC		

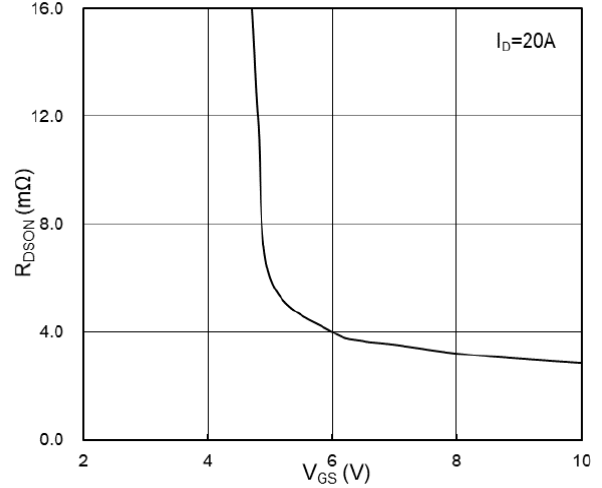
Notes:

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2oz copper.
2. The data tested by pulsed pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .
3. The power dissipation is limited by 150°C junction temperature.
4. The  $E_{AS}$  data shows Max. rating. The test condition is  $V_{DD}=50V, V_{GS}=10V, L=0.1mH, I_{AS}=45A$ .

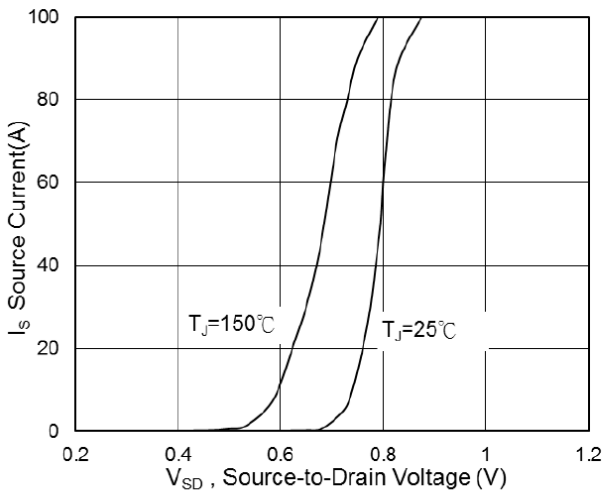
**TYPICAL CHARACTERISTIC**



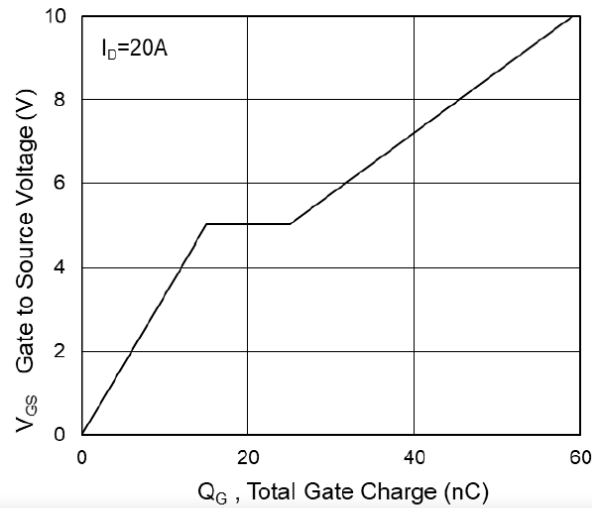
**Fig.1 Typical Output Characteristics**



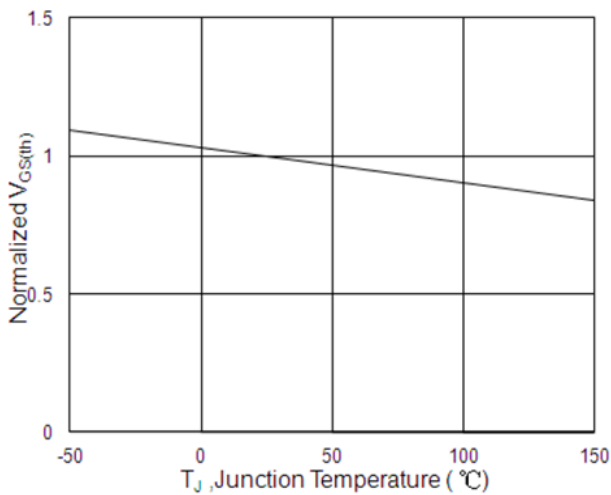
**Fig.2 On-Resistance vs G-S Voltage**



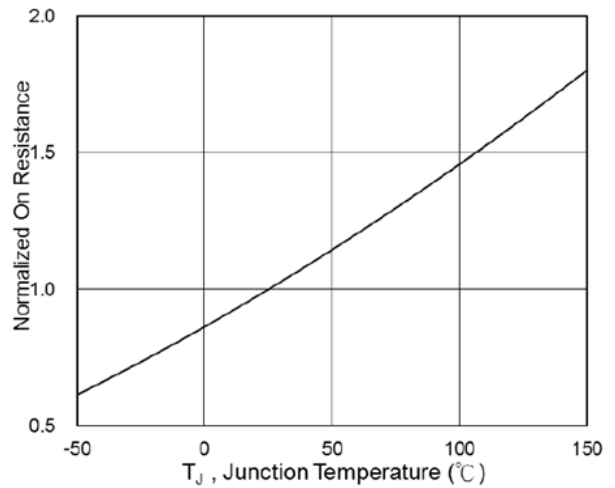
**Fig.3 Diode Forward Voltage vs Current**



**Fig.4 Gate-Charge Characteristics**

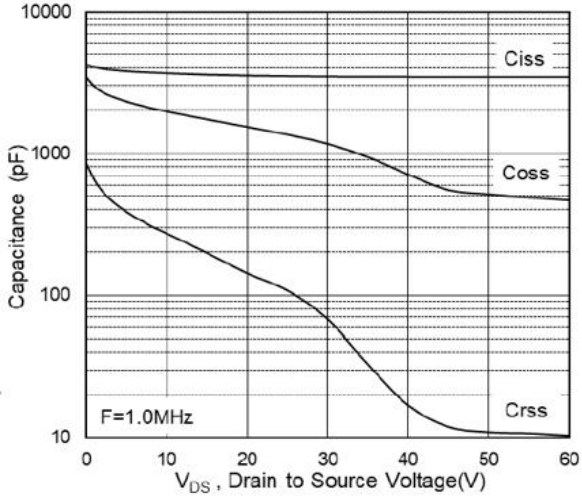


**Fig.5 Normalized  $V_{GS(th)}$  vs  $T_J$**

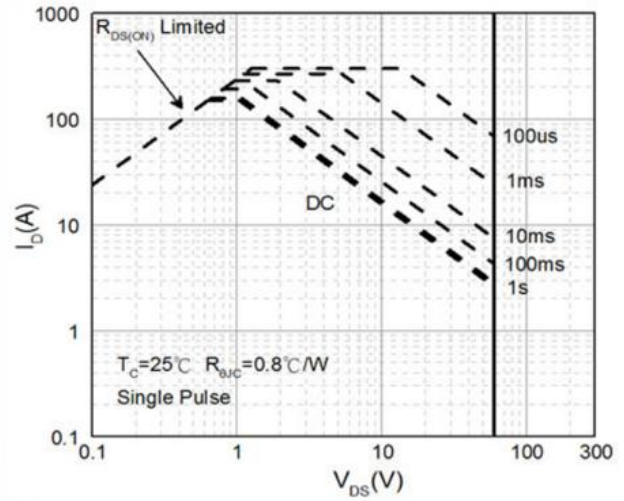


**Fig.6 Normalized  $R_{DS(ON)}$  vs  $T_J$**

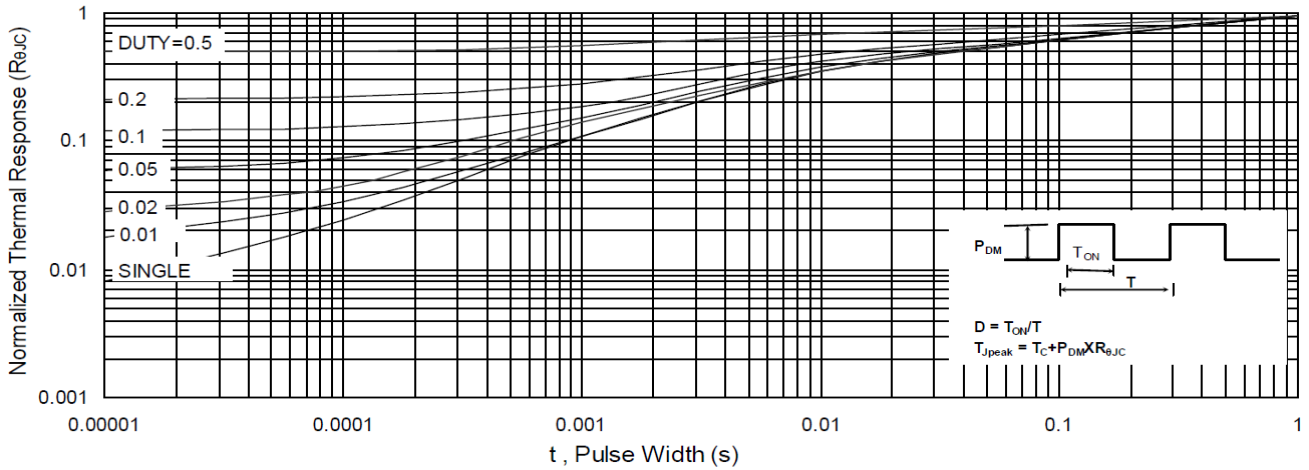
**TYPICAL CHARACTERISTIC**



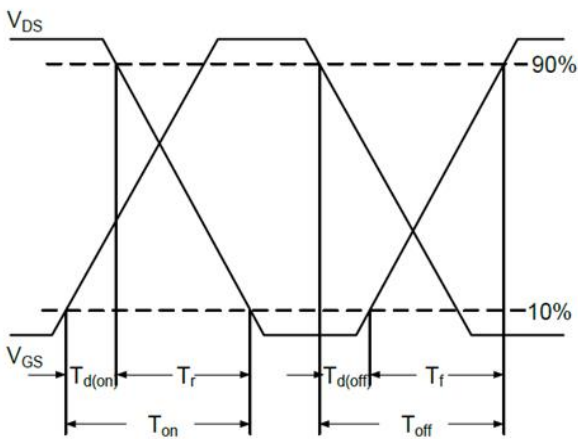
**Fig.7 Capacitance**



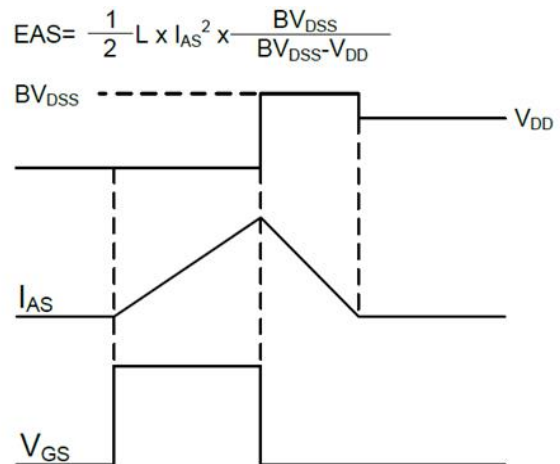
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**