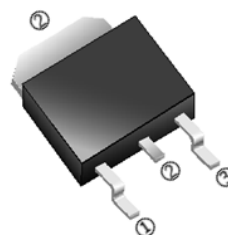


RoHS Compliant Product  
A suffix of "-C" specifies halogen free

## DESCRIPTION

The SSD50N10-C is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent  $R_{DS(on)}$  and gate charge for most of the synchronous buck converter applications.

## TO-252(D-Pack)



## FEATURES

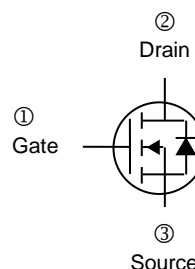
- Advanced High Cell Density Trench Technology
- Super Low Gate Charge
- Excellent CdV/dt Effect Decline
- 100% EAS Guaranteed
- Green Device Available

## MARKING



## PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-252	2.5K	13 inch



## ORDER INFORMATION

Part Number	Type
SSD50N10-C	Lead (Pb)-free and Halogen-free

## ABSOLUTE MAXIMUM RATINGS ( $T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current @ $V_{GS}=10V$ <sup>1</sup>	$I_D$	$T_C=25^\circ\text{C}$	50
		$T_C=100^\circ\text{C}$	28
Pulsed Drain Current <sup>2</sup>	$I_{DM}$	100	A
Total Power Dissipation <sup>4</sup>	$P_D$	$T_C=25^\circ\text{C}$	90
		$T_A=70^\circ\text{C}$	2
Single Pulse Avalanche Energy <sup>3</sup>	$E_{AS}$	98	mJ
Single Pulse Avalanche Current	$I_{AS}$	41	A
Operating Junction & Storage Temperature Range	$T_J, T_{STG}$	-55~150	$^\circ\text{C}$
<b>Thermal Resistance Rating</b>			
Maximum Thermal Resistance Junction-Ambient <sup>1</sup>	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Maximum Thermal Resistance Junction-Case <sup>1</sup>	$R_{\theta JC}$	1.4	

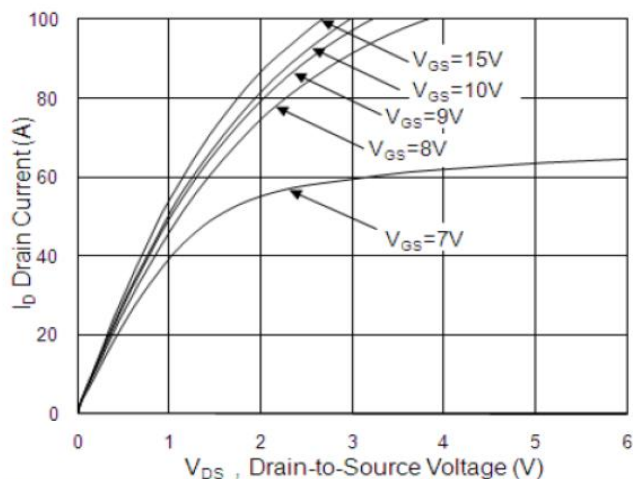
**ELECTRICAL CHARACTERISTICS** ( $T_J=25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Drain-Source Breakdown Voltage	$BV_{DSS}$	100	-	-	V	$V_{GS}=0, I_D=250\mu\text{A}$	
Gate-Threshold Voltage	$V_{GS(th)}$	2	-	4.5	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	
Gate-Source Leakage Current	$I_{GSS}$	-	-	$\pm 100$	nA	$V_{GS}=\pm 20\text{V}$	
Drain-Source Leakage Current	$I_{DSS}$	$T_J=25^\circ\text{C}$	-	-	1	$\mu\text{A}$	$V_{DS}=80\text{V}, V_{GS}=0$
		$T_J=55^\circ\text{C}$	-	-	5		
Static Drain-Source On-Resistance <sup>2</sup>	$R_{DS(ON)}$	-	18	22	m $\Omega$	$V_{GS}=10\text{V}, I_D=30\text{A}$	
Gate Resistance	$R_g$	-	1.9	3.8	$\Omega$	$f=1\text{MHz}$	
Total Gate Charge <sup>2</sup>	$Q_g$	-	34.3	-	nC	$I_D=30\text{A}$ $V_{DS}=80\text{V}$ $V_{GS}=10\text{V}$	
Gate-Source Charge	$Q_{gs}$	-	14.8	-			
Gate-Drain ("Miller") Change	$Q_{gd}$	-	11.5	-			
Turn-on Delay Time <sup>2</sup>	$T_{d(on)}$	-	15.4	-	nS	$V_{DD}=50\text{V}$ $I_D=30\text{A}$ $V_{GS}=10\text{V}$ $R_G=3.3\Omega$	
Rise Time	$T_r$	-	83	-			
Turn-off Delay Time	$T_{d(off)}$	-	18	-			
Fall Time	$T_f$	-	33.3	-			
Input Capacitance	$C_{iss}$	-	2078	-	pF	$V_{GS}=0$ $V_{DS}=15\text{V}$ $f=1\text{MHz}$	
Output Capacitance	$C_{oss}$	-	285	-			
Reverse Transfer Capacitance	$C_{rss}$	-	94	-			
Single Pulse Avalanche Energy <sup>5</sup>	$E_{AS}$	53	-	-	mJ	$V_{DD}=25\text{V}, L=0.1\text{mH}, I_{AS}=30\text{A}$	
<b>Source-Drain Diode</b>							
Diode Forward Voltage <sup>2</sup>	$V_{SD}$	-	-	1.2	V	$I_S=1\text{A}, V_{GS}=0, T_J=25^\circ\text{C}$	
Continuous Source Current <sup>1 6</sup>	$I_S$	-	-	45	A	$V_D=V_G=0, \text{Force Current}$	
Pulsed Source Current <sup>2 6</sup>	$I_{SM}$	-	-	100	A		
Reverse Recovery Time	$T_{rr}$	-	34	-	nS	$I_F=30\text{A}, dI/dt=100\text{A}/\mu\text{s},$ $T_J=25^\circ\text{C}$	
Reverse Recovery Charge	$Q_{rr}$	-	47	-	nC		

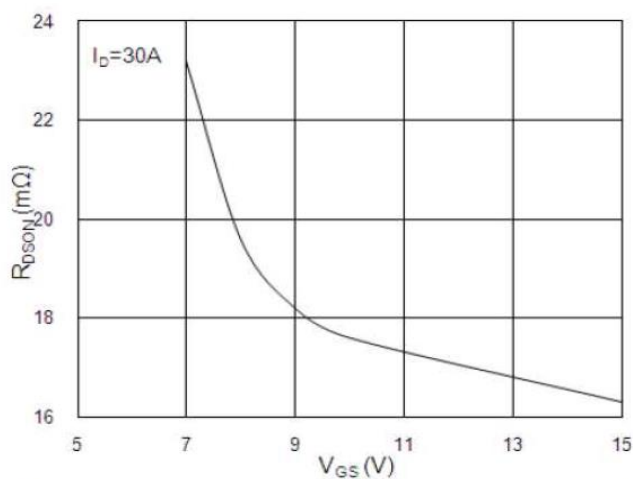
Notes:

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2oz copper.
2. The data tested by pulsed, pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .
3. The  $E_{AS}$  data shows Max. rating. The test condition is  $V_{DD}=25\text{V}, V_{GS}=10\text{V}, L=0.1\text{mH}, I_{AS}=41\text{A}$ .
4. The power dissipation is limited by  $150^\circ\text{C}$ , junction temperature.
5. The Min. value is 100%  $E_{AS}$  tested guarantee.
6. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.

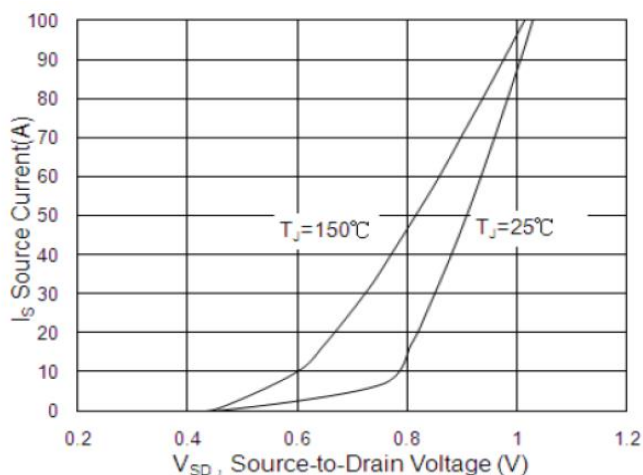
**CHARACTERISTIC CURVES**



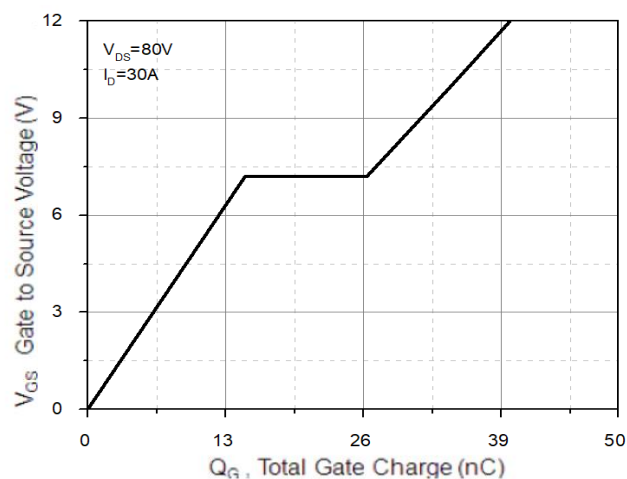
**Fig.1 Typical Output Characteristics**



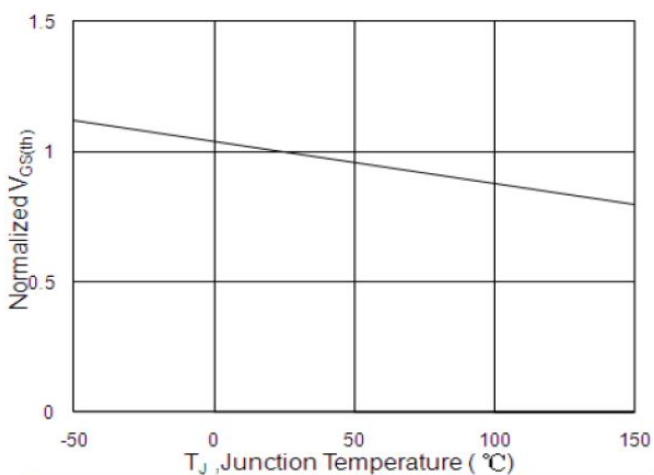
**Fig.2 On-Resistance v.s Gate-Source**



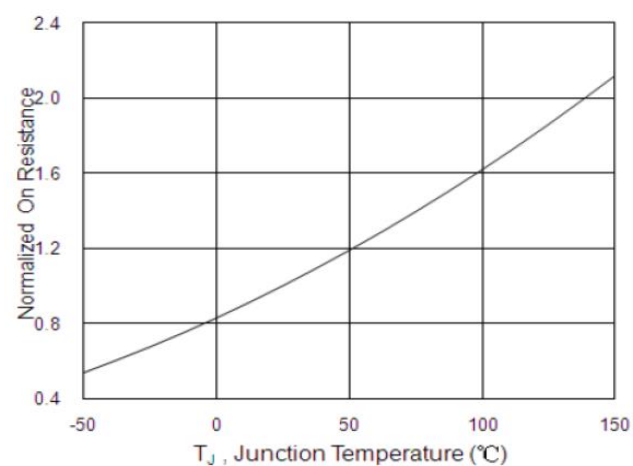
**Fig.3 Forward Characteristics of Reverse**



**Fig.4 Gate-Charge Characteristics**

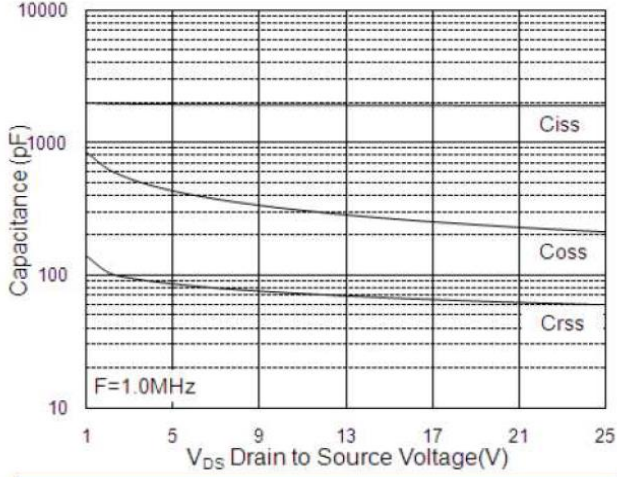


**Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_J$**

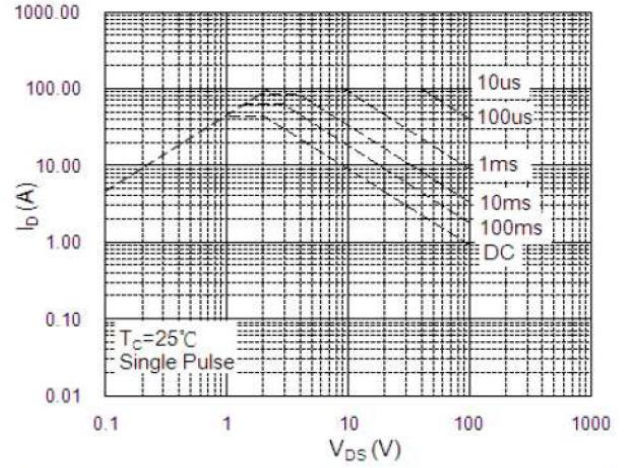


**Fig.6 Normalized  $R_{DS(on)}$  v.s  $T_J$**

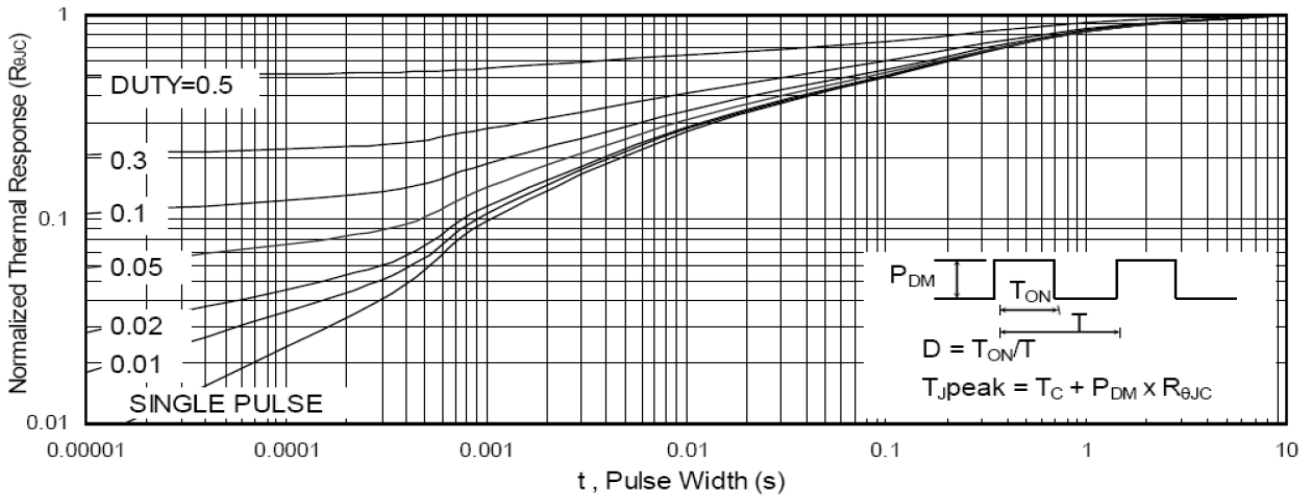
**CHARACTERISTIC CURVES**



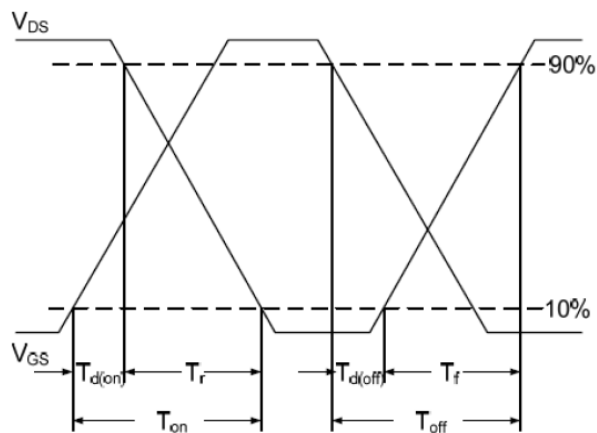
**Fig.7 Capacitance**



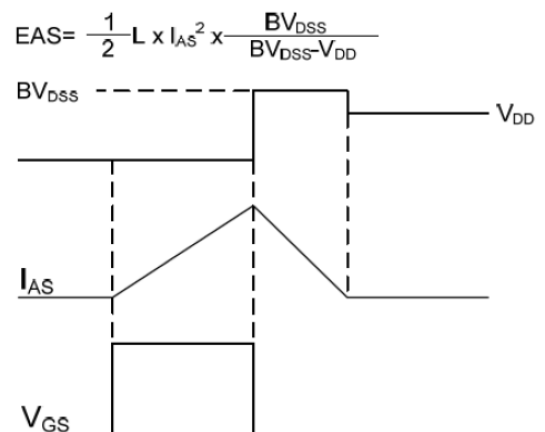
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



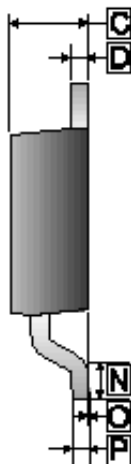
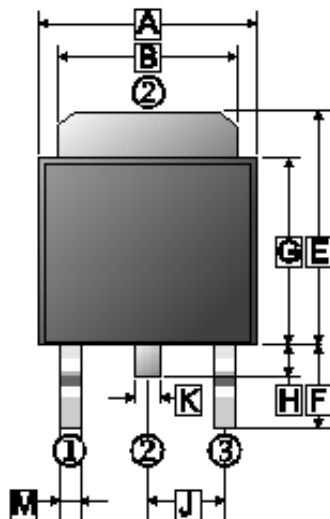
**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Wave**

**PACKAGE OUTLINE DIMENSIONS**

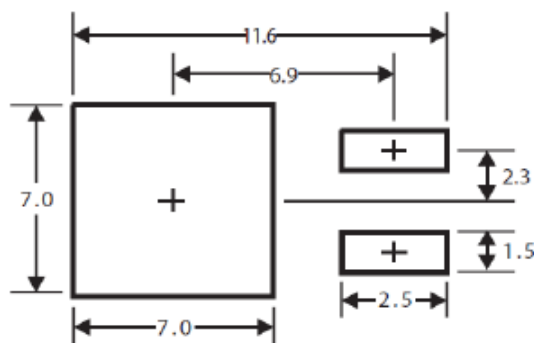
TO-252



REF.	Millimeter	
	Min.	Max.
A	6.30	6.90
B	4.95	5.53
C	2.10	2.50
D	0.40	0.90
E	6.00	7.70
F	2.90 REF.	
G	5.40	6.40
H	0.60	1.20
J	2.30 REF.	
K	0.89 REF.	
M	0.45	1.14
N	1.55 TYP.	
O	0	0.15
P	0.58 REF.	

**MOUNTING PAD LAYOUT**

TO-252



\*Dimensions in millimeters