Elektronische Bauelemente

SSD9435-C

-20A, -30V, $R_{DS(ON)}$ 50mΩ
P-Ch Enhancement Mode Power MOSFET

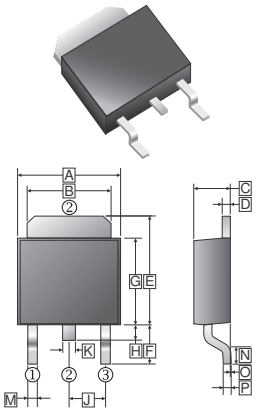
RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

SSD9435-C is the highest performance trench P-ch MOSFETs with extreme high cell density, which provides excellent $R_{DS(ON)}$ and gate charge for most synchronous buck converter applications.

SSD9435-C meets the RoHS and Green Product requirement, 100% E_{AS} guaranteed with full function reliability approved.

TO-252(D-Pack)



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.35	6.9	J	2.3 REF.	
B	4.95	5.53	K	0.89 REF.	
C	2.1	2.5	M	0.45	1.14
D	0.41	0.9	N	1.55 TYP.	
E	6	7.5	O	0	0.13
F	2.90 REF		P	0.58 REF.	
G	5.4	6.4			
H	0.6	1.2			

FEATURES

- Advanced High Cell Density Trench Technology
- Super Low Gate Charge
- 100% E_{AS} Guaranteed

APPLICATIONS

- Power switching applications
- Hard switched and high frequency circuits
- Uninterruptible power supply

MARKING

9435
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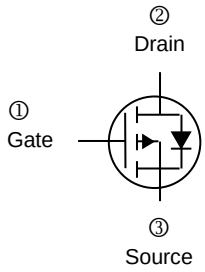


PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-252	2.5K	13 inch

ORDER INFORMATION

Part Number	Type
SSD9435-C	Lead (Pb)-free and Halogen-free

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current @V_{GS}=10V [1]	T_C=25℃	I_D	-20	A
	T_C=100℃		-13	
	T_A=25℃		-5.8	
	T_A=70℃		-4.6	
Pulsed Drain Current [2]		I_{DM}	-40	A
Single Pulse Avalanche Energy [3]		E_{AS}	18	mJ
Avalanche Current		I_{AS}	-19	A
Total Power Dissipation [4]	T_C=25℃	P_D	25	W
	T_A=25℃		2	W
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55 ~ 150	℃
Thermal Resistance Ratings				
Thermal Resistance from Junction-Ambient [1]		$R_{\theta JA}$	62	℃/W
Thermal Resistance from Junction-Ambient		$R_{\theta JA}$	110	
Thermal Resistance from Junction-Case [1]		$R_{\theta JC}$	5	

ELECTRICAL CHARACTERISTICS (T_J=25℃ unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain-Source Breakdown Voltage		BV_{DSS}	-30	-	-	V	V_{GS}=0, I_D= -250μA
Gate Threshold Voltage		$V_{GS(th)}$	-1	-	-2.5	V	V_{DS}=V_{GS}, I_D= -250μA
Forward Transfer conductance		gfs	-	12	-	S	V_{DS}= -5V, I_D= -15A
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{DS}=0V, V_{GS}= ±20V
Drain-Source Leakage Current	T_J=25℃	I_{DSS}	-	-	-1	μA	V_{DS}= -24V, V_{GS}=0
	T_J=55℃		-	-	-5		V_{DS}= -24V, V_{GS}=0
Static Drain-Source On-Resistance [2]		$R_{DS(ON)}$	-	-	50	mΩ	V_{GS}= -10V, I_D= -15A
			-	-	90		V_{GS}= -4.5V, I_D= -10A
Total Gate Charge		Q_g	-	6.1	-	nC	V_{DS}= -15V V_{GS}= -4.5V I_D= -15A
Gate-Source Charge		Q_{gs}	-	3.1	-		
Gate-Drain (“Miller”) Charge		Q_{gd}	-	1.8	-		
Turn-on Delay Time		$T_{d(on)}$	-	2.6	-	nS	V_{DD}= -15V V_{GS}= -10V R_G=3.3Ω I_D= -15A
Rise Time		T_r	-	8.6	-		
Turn-off Delay Time		$T_{d(off)}$	-	33.6	-		
Fall Time		T_f	-	6	-		
Input Capacitance		C_{iss}	-	585	-	pF	V_{DS}= -15V V_{GS}=0 f=1MHz
Output Capacitance		C_{oss}	-	100	-		
Reverse Transfer Capacitance		C_{rss}	-	85	-		
Guaranteed Avalanche Characteristics							
Single Pulse Avalanche Energy [5]		E_{AS}	5	-	-	mJ	V_{DD}= -25V, L=0.1mH, I_{AS}= -10A
Source-Drain Diode Characteristics							
Diode Forward Voltage [2]		V_{SD}	-	-	-1.2	V	I_S= -1A, V_{GS}=0
Continuous Source Current [1 6]		I_S	-	-	-20	A	V_G=V_D=0V, Force Current
Pulsed Source Current [2 6]		I_{SM}	-	-	-40		

Notes:

1. The data is tested with the surface of the device is mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2. The data is tested by pulse: Pulse width≦300μs, duty cycle≦2%.
3. The E_{AS} data shows maximum rating. The test condition is V_{DD}= -25V, V_{GS}= -10V, L=0.1mH, I_{AS}= -19A.
4. The power dissipation is limited by 150℃ junct ion temperature.
5. The minimum value is 100% E_{AS} tested guarantee.
6. The data is theoretically the same as I_D and I_{DM}. In real applications, the data should be limited by the total power dissipation.

CHARACTERISTIC CURVE

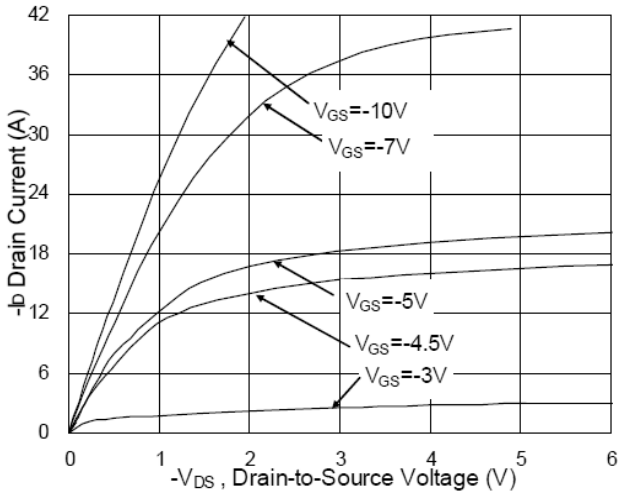


Fig.1 Typical Output Characteristics

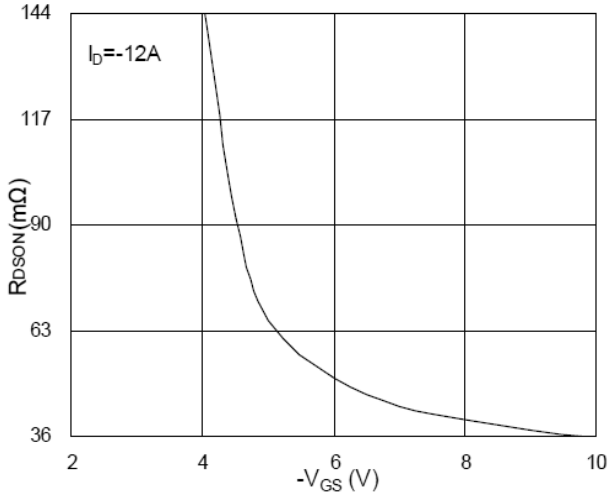


Fig.2 On-Resistance v.s Gate-Source

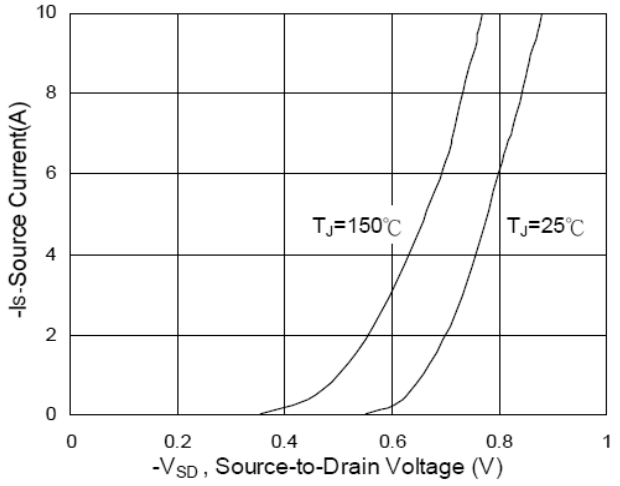


Fig.3 Forward Characteristics Of Reverse

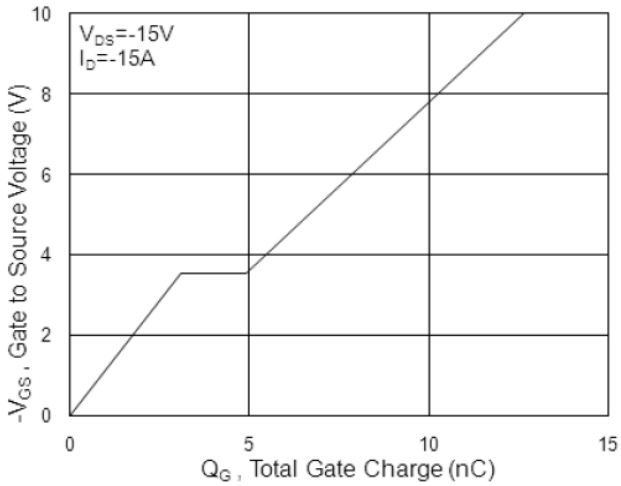


Fig.4 Gate Charge Characteristics

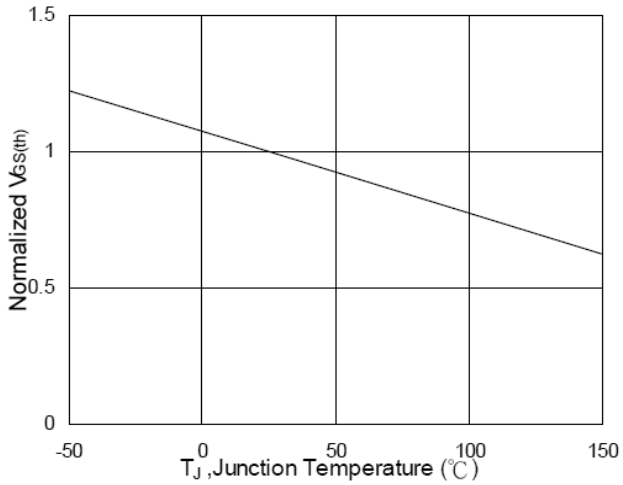


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

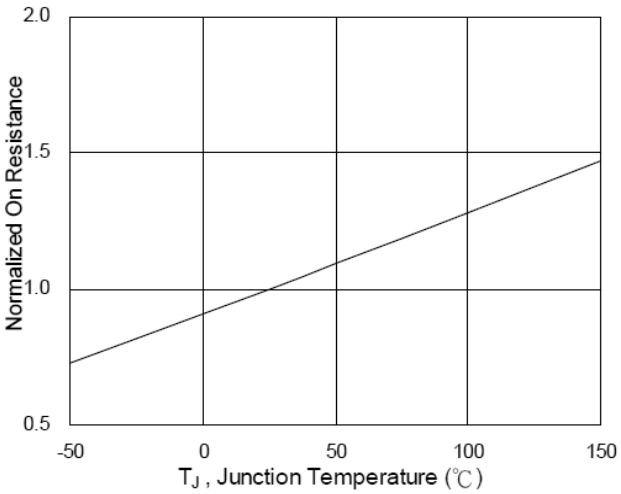


Fig.6 Normalized R_{DSON} vs. T_J

CHARACTERISTIC CURVE

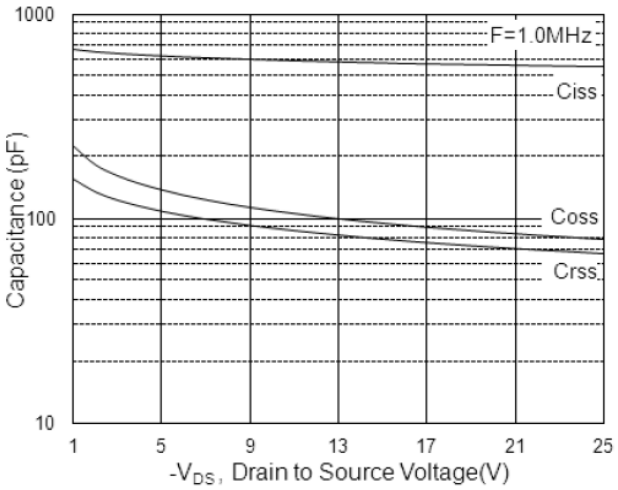


Fig.7 Capacitance

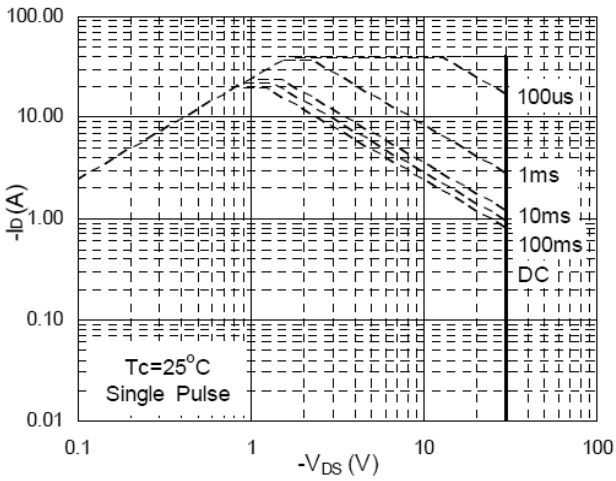


Fig.8 Safe Operating Area

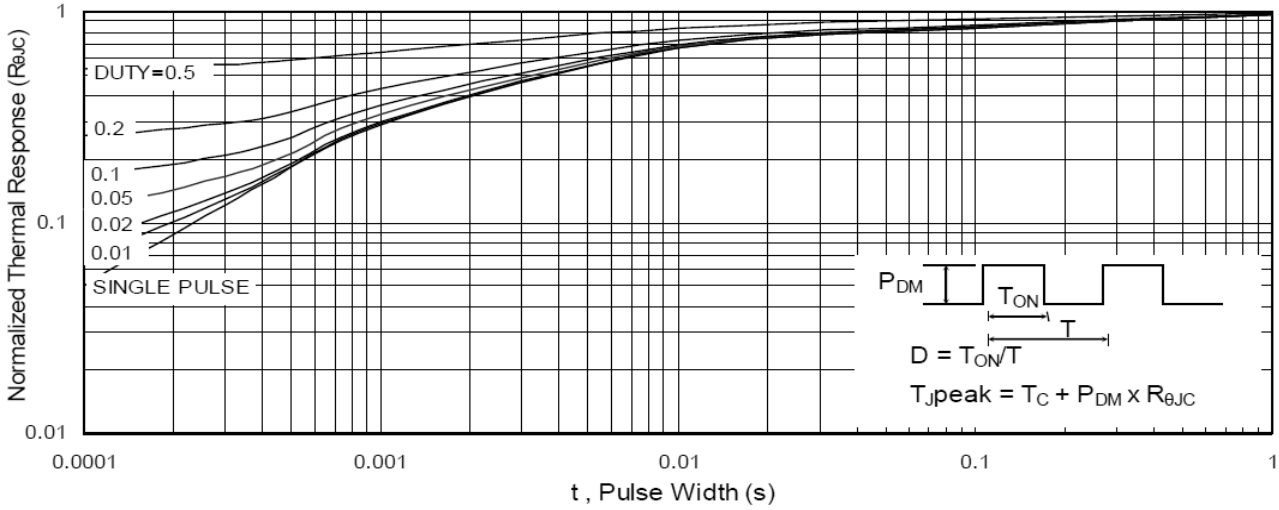


Fig.9 Normalized Maximum Transient Thermal Impedance

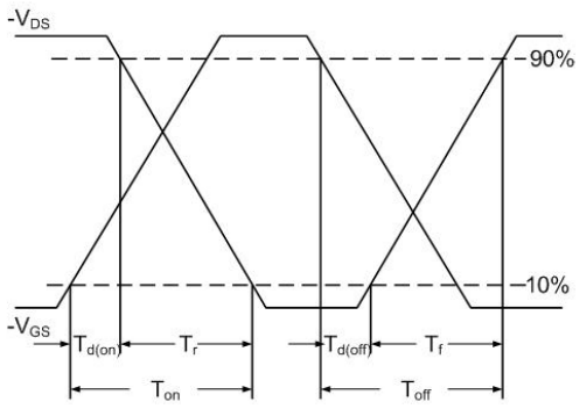


Fig.10 Switching Time Waveform

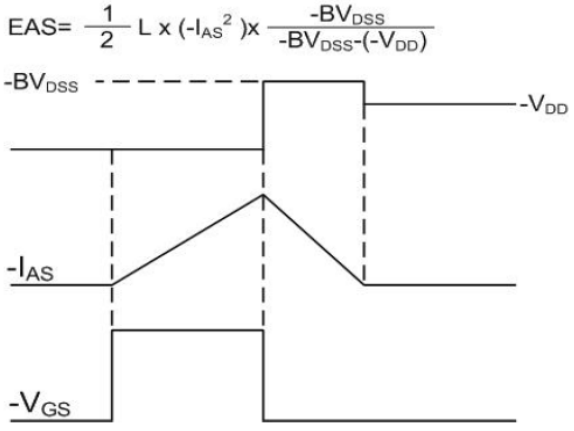
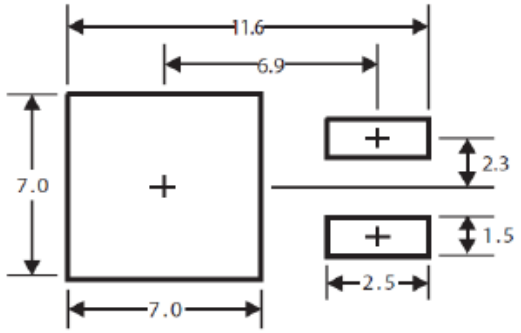


Fig.11 Unclamped Inductive Switching Waveform

CHARACTERISTIC CURVE



*Dimensions in millimeters

Fig.12 Mounting Pad Layout