Elektronische Bauelemente

SSU40N01

149A , 40V , $R_{DS(ON)}$ 2.2mΩ

N-Ch Enhancement Mode Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen free

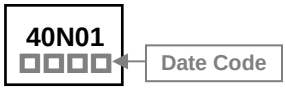
DESCRIPTION

The SSU40n01 is the highest performance trench N-ch MOSFETs with extreme high cell density , which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications .

FEATURES

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS and 100% Rg Guaranteed
- Green Device Available

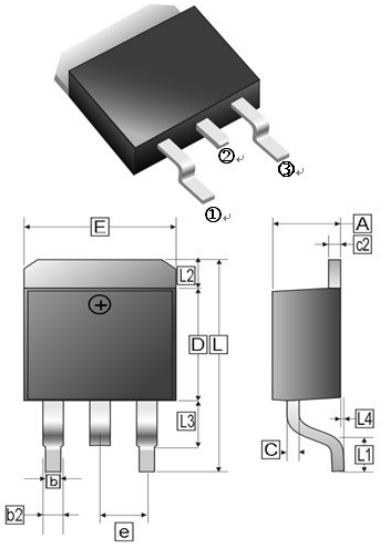
MARKING

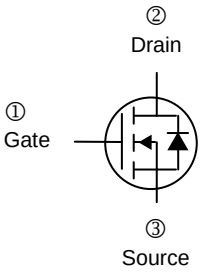


PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-263	0.8K	13 inch

TO-263





REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.40	4.80	c2	1.17	1.45
b	0.76	1.00	b2	1.1	1.47
L4	0.00	0.30	D	8.5	9.0
c	0.36	0.5	e	2.54 REF	
L3	1.50 REF		L	14.6	15.8
L1	2.29	2.79	θ	0°	8°
E	9.80	10.4	L2	1.27 REF	

ABSOLUTE MAXIMUM RATINGS (T_A=25℃ unless otherwise specified)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1]	T_C=25℃	I_D	149	A
	T_C=70℃		119	
	T_A=25℃		30	
	T_A=70℃		24	
Pulsed Drain Current [1]		I_{DM}	480	A
Total Power Dissipation	T_C=25℃	P_D	83	W
	T_A=25℃		2	
Single Pulse Avalanche Energy, L=0.1mH		E_{AS}	201	mJ
Single Pulse Avalanche Current, L=0.1mH		I_{AS}	63.5	A
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	℃
Thermal Resistance Rating				
Maximum Thermal Resistance Junction-Ambient [2]		$R_{\theta JA}$	62	℃ / W
Maximum Thermal Resistance Junction-Case [2]		$R_{\theta JC}$	1.5	℃ / W

ELECTRICAL CHARACTERISTICS (T_J=25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	40	-	-	V	V_{GS}=0, I_D=250μA
Gate-Threshold Voltage	$V_{GS(th)}$	2	3	4	V	V_{DS}=V_{GS}, I_D=250μA
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current	I_{DSS}	-	-	1	μA	V_{DS}=32V, V_{GS}=0
Static Drain-Source On-Resistance [2]	$R_{DS(ON)}$	-	1.9	2.2	mΩ	V_{GS}=10V, I_D=30A
Total Gate Charge	Q_g	-	78.8	-	nC	I_D=30A V_{DS}=20V V_{GS}=10V
Gate-Source Charge	Q_{gs}	-	23	-		
Gate-Drain (“Miller”) Change	Q_{gd}	-	4.85	-		
Turn-on Delay Time	$T_{d(on)}$	-	21	-	nS	V_{DS}=20V I_D=30A V_{GS}=10V R_G=3Ω
Rise Time	T_r	-	6	-		
Turn-off Delay Time	$T_{d(off)}$	-	98	-		
Fall Time	T_f	-	17	-		
Input Capacitance	C_{iss}	-	4222	-	pF	V_{GS} =0 V_{DS}=20V f =1.0MHz
Output Capacitance	C_{oss}	-	889	-		
Reverse Transfer Capacitance	C_{rss}	-	398	-		
Guaranteed Avalanche Characteristics						
Single Pulse Avalanche Energy [3]	EAS	110	-	-	mJ	V_{DD}=20V,L=0.1mH , I_{AS}=47A
Source-Drain Diode						
Diode Forward Voltage	V_{SD}	-	-	1.3	V	I_S=30A, V_{GS}=0
Reverse Recovery Time	T_{rr}	-	32	-	ns	I_F=30A, T_J = 25℃ dI/dt=100A/μs
Reverse Recovery Charge	Q_{rr}	-	120	-	nC	

Notes:
1. The data tested by pulsed, pulse width ≦ 300us, duty cycle ≦ 2%.
2. RθJA is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. RθJC is guaranteed by design while RθCA is determined by the user's board design. RθJA shown below for single device operation on FR-4 in still air.
3. The Min. value is 100% EAS tested guarantee

CHARACTERISTIC CURVES

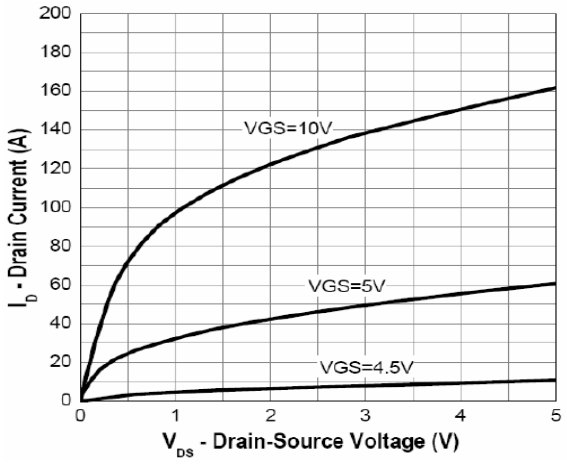


Fig.1 Typical Output Characteristics

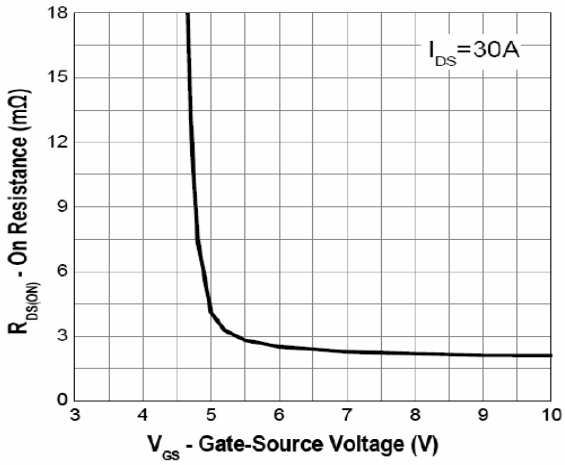


Fig.2 On-Resistance vs. G-S Voltage

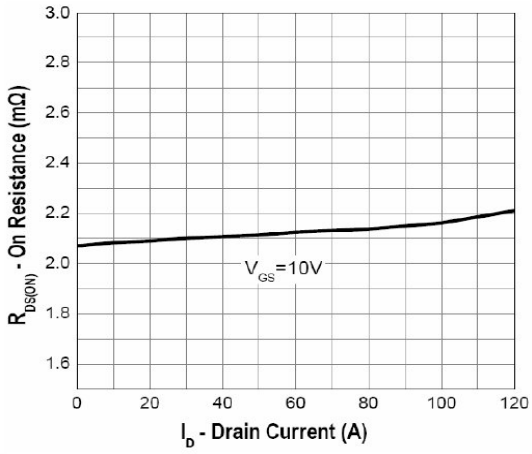


Fig.3 On-Resistance vs. Drain Current

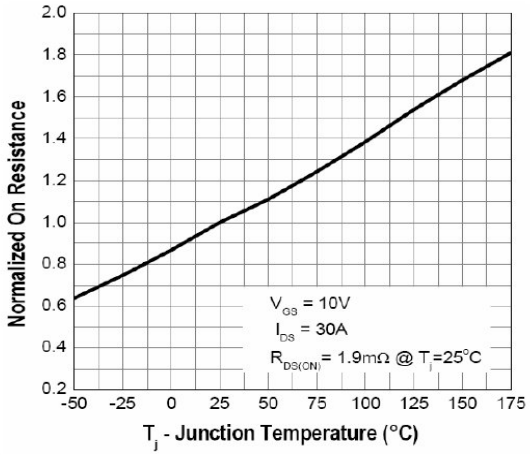


Fig.4 Normalized R_{DSON} vs. T_J

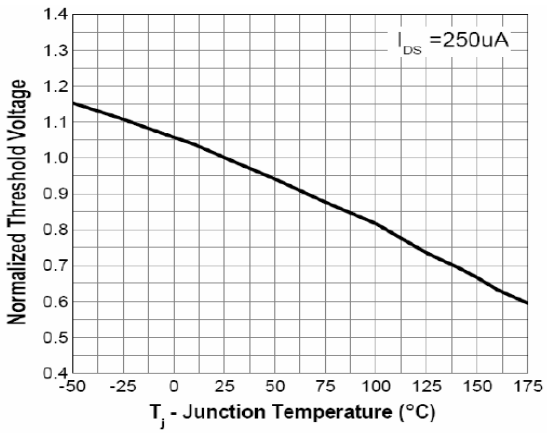


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

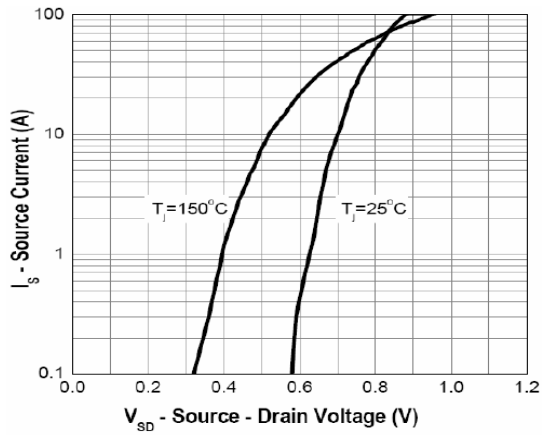


Fig.6 Forward Characteristics of Reverse

CHARACTERISTIC CURVES

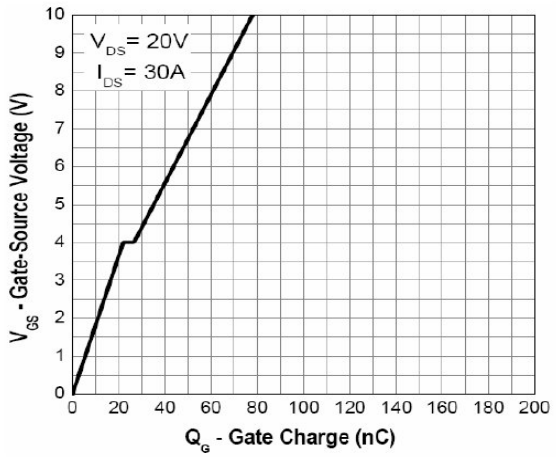


Fig.7 Gate Charge Characteristics

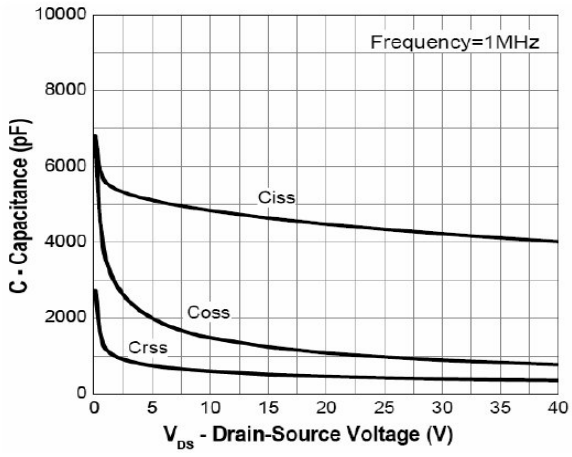


Fig.8 Capacitance Characteristic

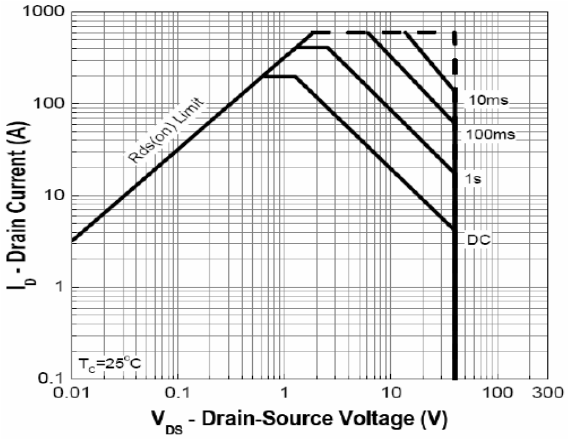


Fig.9 Safe Operating Area

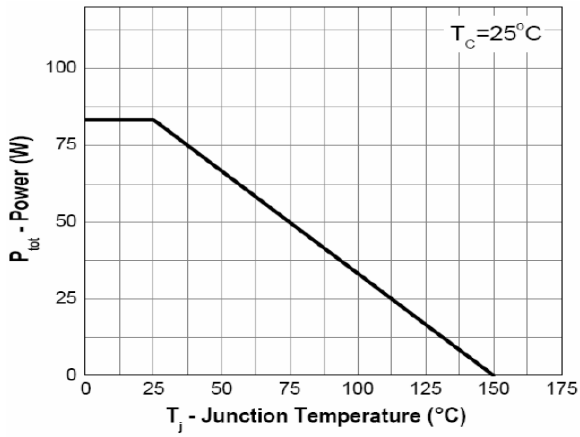


Fig.10 Power Dissipation

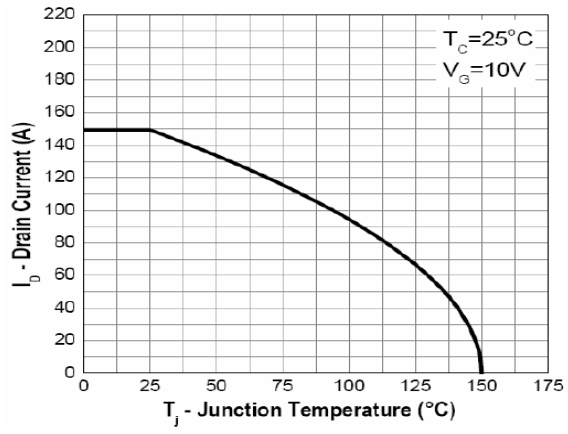


Fig.11 Drain Current vs. T_J

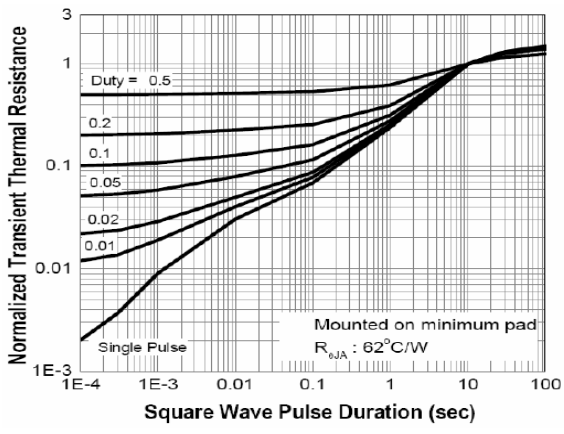


Fig.12 Transient Thermal Impedance