

RoHS Compliant Product
A suffix of "-C" specifies halogen and lead-free

DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide Low $R_{DS(ON)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

FEATURES

- Low $R_{DS(ON)}$ Provides Higher Efficiency and Extends Battery Life
- Low Thermal Impedance Copper Lead Frame TSOP-6 Saves Board Space
- Fast Switching Speed
- High Performance Trench Technology

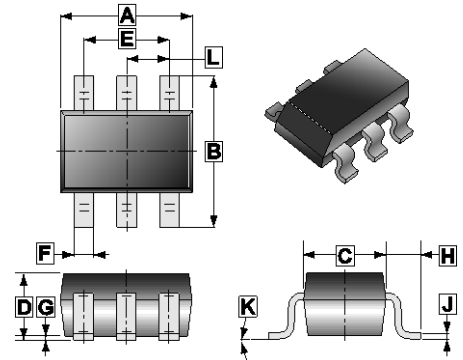
PACKAGE INFORMATION

Package	MPQ	Leader Size
TSOP-6	3K	7 inch

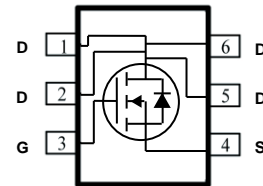
ORDER INFORMATION

Part Number	Type
STT3434N-C	Lead (Pb)-free and Halogen-free

TSOP-6



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	0	0.10
B	2.60	3.00	H	0.60	REF.
C	1.40	1.80	J	0.12	REF.
D	1.10	Max.	K	0°	10°
E	1.90	REF.	L	0.95	REF.
F	0.30	0.50			



ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 12	V
Continuous Drain Current ¹	I_D	$T_A=25^\circ\text{C}$	6.5
		$T_A=70^\circ\text{C}$	5.3
Pulsed Drain Current ²	I_{DM}	25	A
Continuous Source Current (Diode Conduction) ¹	I_S	2.9	A
Power Dissipation ¹	P_D	$T_A=25^\circ\text{C}$	2
		$T_A=70^\circ\text{C}$	1.3
Operating Junction & Storage Temperature Range	T_J, T_{STG}	-55~150	$^\circ\text{C}$
Thermal Resistance Ratings			
Maximum Thermal Resistance from Junction-Ambient ¹	$R_{\theta JA}$	$\leq 10\text{sec}$	62.5
		Steady State	110
Maximum Thermal Resistance from Junction-Case ¹	$R_{\theta JC}$	70	$^\circ\text{C/W}$

Notes:

1. The surface of the device is mounted on a 1" x 1" FR-4 Board.
2. The pulse width is limited by the maximum junction temperature.

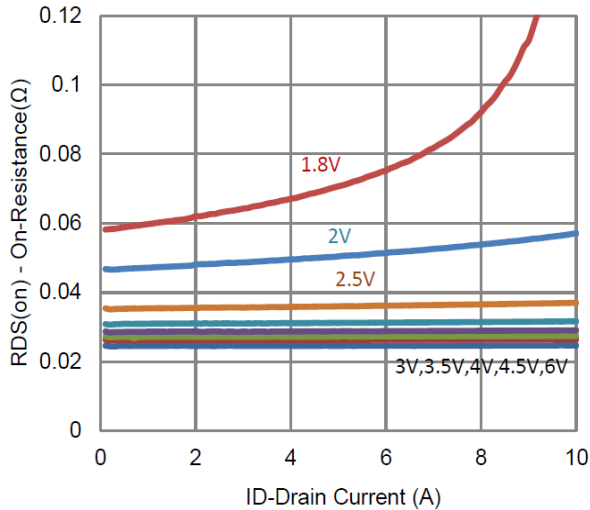
ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Gate-Threshold Voltage	$V_{GS(th)}$	0.4	-	-	V	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$
Forward Transconductance ¹	g_{fs}	-	8	-	S	$V_{DS}=15\text{V}$, $I_D=2\text{A}$
Gate-Body Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{DS}=0\text{V}$, $V_{GS}= \pm 12\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1	μA	$V_{DS}=24\text{V}$, $V_{GS}=0$
		-	-	10		$V_{DS}=24\text{V}$, $V_{GS}=0$, $T_J=55^\circ\text{C}$
On-State Drain Current ¹	$I_{D(on)}$	9	-	-	A	$V_{DS}=5\text{V}$, $V_{GS}=4.5\text{V}$
Drain-Source On-Resistance ¹	$R_{DS(ON)}$	-	-	32	m Ω	$V_{GS}=4.5\text{V}$, $I_D=2\text{A}$
		-	-	40		$V_{GS}=2.5\text{V}$, $I_D=1.6\text{A}$
Total Gate Charge	Q_g	-	9	-	nC	$V_{DS}=15\text{V}$ $V_{GS}=4.5\text{V}$ $I_D=2\text{A}$
Gate-Source Charge	Q_{gs}	-	1.7	-		
Gate-Drain Charge	Q_{gd}	-	3	-		
Turn-on Delay Time	$T_{d(on)}$	-	10	-	nS	$V_{DS}=15\text{V}$ $V_{GEN}=4.5\text{V}$ $R_L=7.5\Omega$ $R_{GEN}=6\Omega$ $I_D=2\text{A}$
Rise Time	T_r	-	17	-		
Turn-off Delay Time	$T_{d(off)}$	-	40	-		
Fall Time	T_f	-	11	-		
Input Capacitance	C_{iss}	-	640	-	pF	$V_{GS}=0$ $V_{DS}=15\text{V}$ $f=1\text{MHz}$
Output Capacitance	C_{oss}	-	52	-		
Reverse Transfer Capacitance	C_{rss}	-	46	-		
Source-Drain Diode						
Diode Forward Voltage ¹	V_{SD}	-	0.67	-	V	$I_S=1.5\text{A}$, $V_{GS}=0$

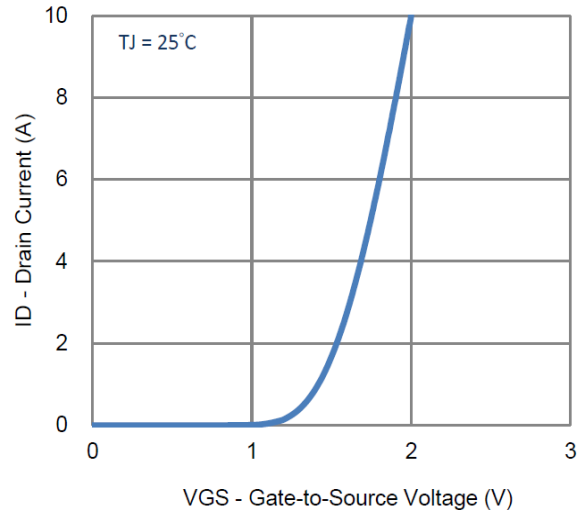
Note:

1. Pulse test: Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.

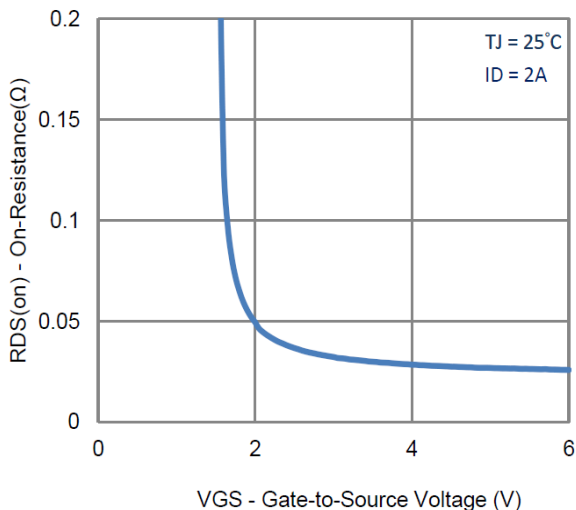
CHARACTERISTICS CURVE



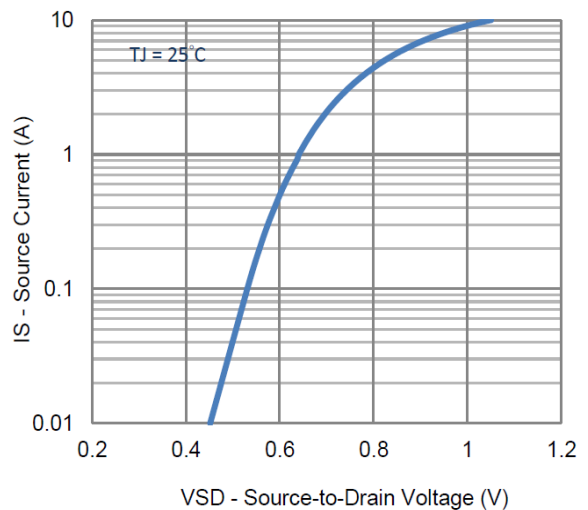
1. On-Resistance vs. Drain Current



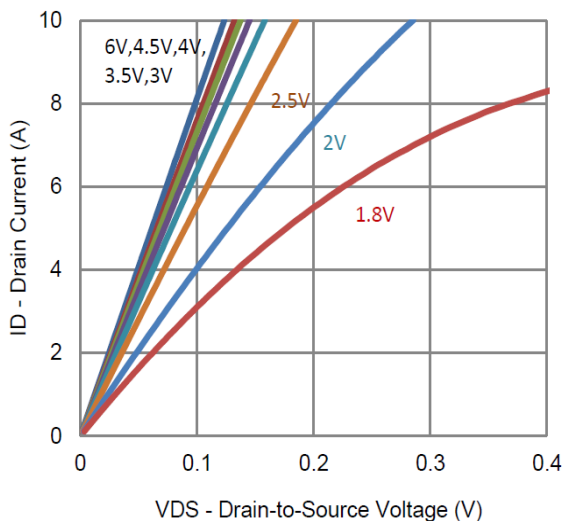
2. Transfer Characteristics



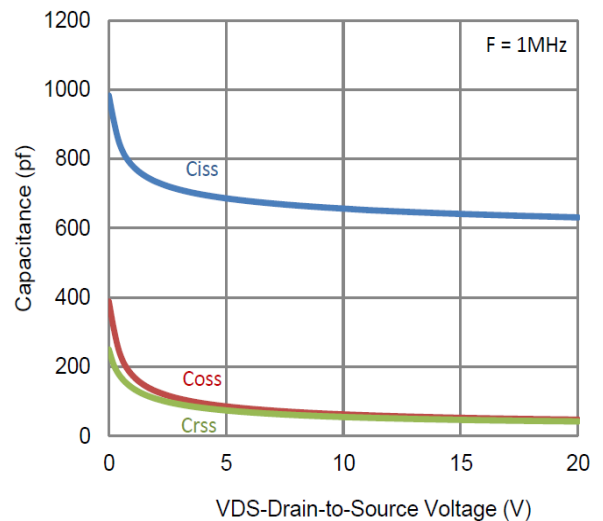
3. On-Resistance vs. Gate-to-Source Voltage



4. Drain-to-Source Forward Voltage

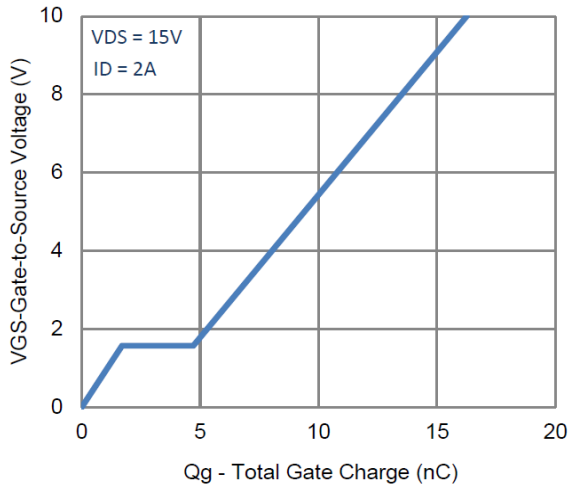


5. Output Characteristics

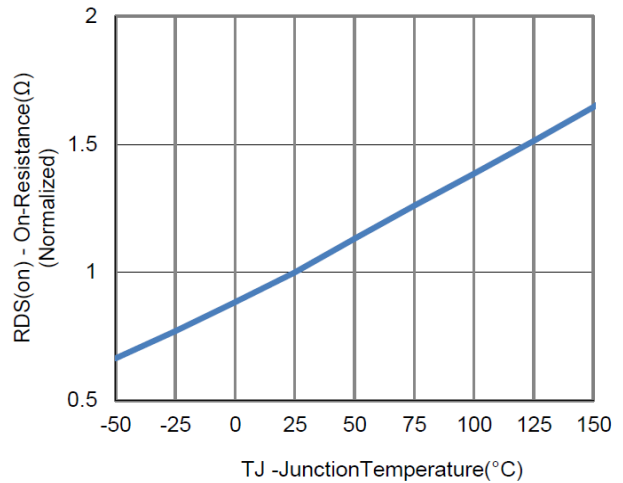


6. Capacitance

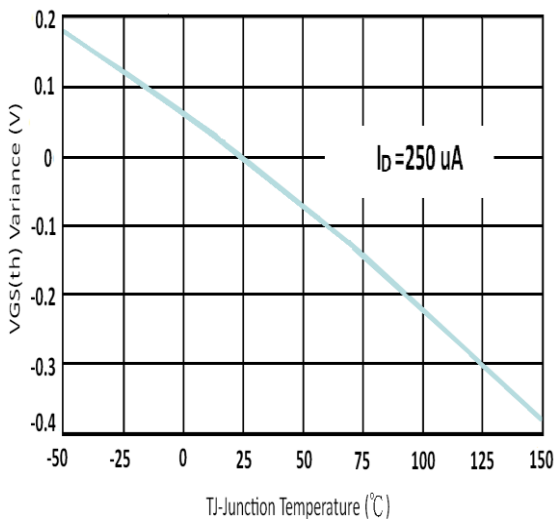
CHARACTERISTICS CURVE



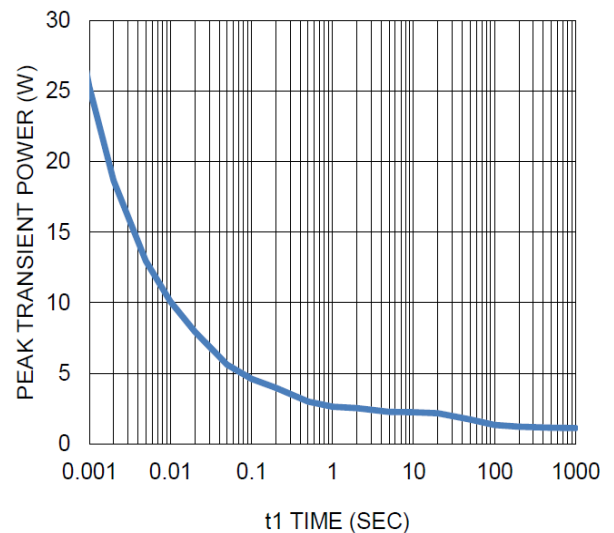
7. Gate Charge



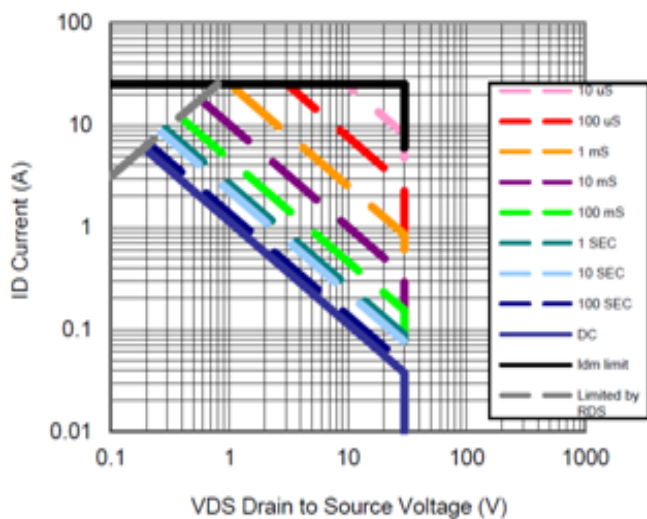
8. Normalized On-Resistance Vs Junction Temperature



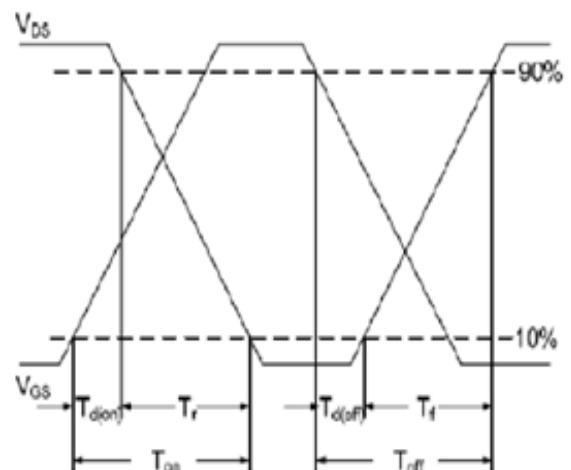
9. VGS(th) Variance vs. TJ



10. Single Pulse Maximum Power Dissipation

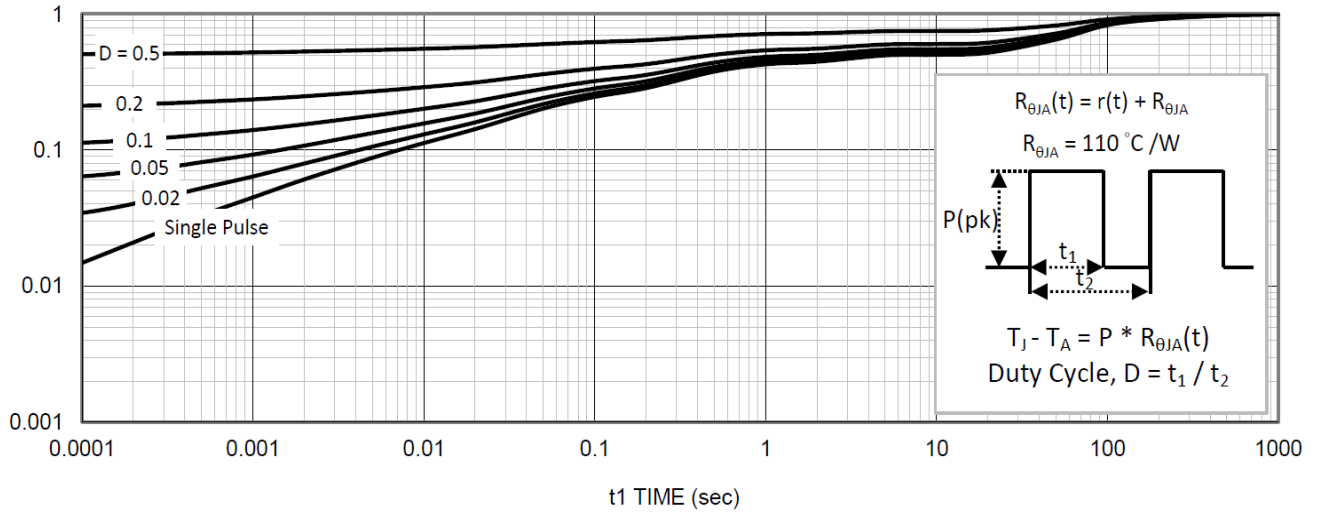


11. Safe Operating Area

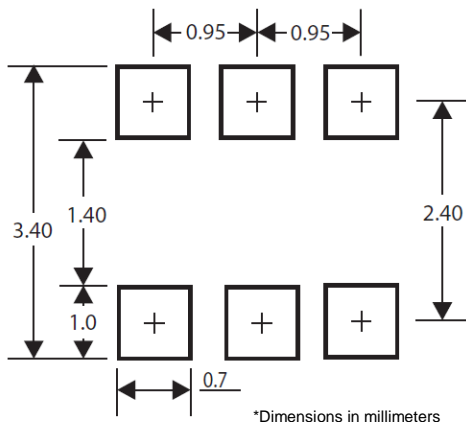


12. Switching Time Waveform

CHARACTERISTICS CURVE



13. Normalized Thermal Transient Junction to Ambient



14. Mounting Pad Layout