Elektronische Bauelemente

KS3V3ULK4-C

56W, 3.3V

Ultra Low Capacitance ESD Protection Array

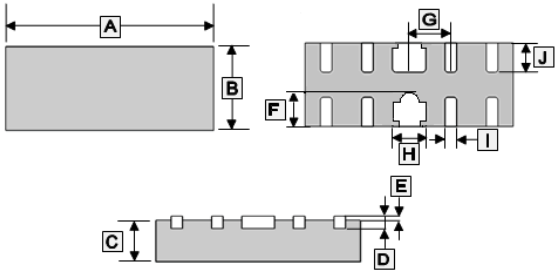
RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

KS3V3ULK4-C is an ultra-low capacitance TVS designed to protection for high-speed data interfaces. With typical capacitance of 0.2pF only, KS3V3ULK4-C is designed to protest parasitic-sensitive systems against over-voltage and over-current transient events.

KS3V3ULK4-C uses ultra-small DFN2510 package. Each KS3V3ULK4-C device can protect four high-speed data lines. The combined features of ultra-low capacitance, ultra-small size and high ESD robustness make KS3V3ULK4-C ideal for high-speed data ports and high-frequency lines (e.g., HDMI &DVI) applications. The low clamping voltage of the KS3V3ULK4-C guarantees a minimum stress on the protected IC.

DFN2510

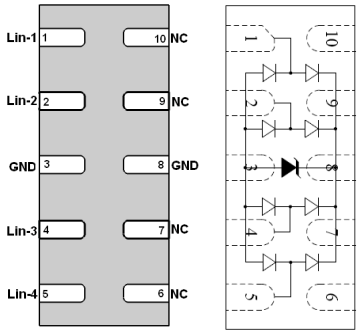


REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.40	2.60	F	0.30	0.50
B	0.90	1.10	G	0.500 BSC.	
C	0.50TYP.		H	0.3	0.5
D	0.150 REF.		I	0.15	0.25
E	0.00	0.05	J	0.30	0.50

FEATURES

- Transient protection for high-speed data lines
- IEC61000-4-2 Level 4 ESD Protection
- Protects four data lines
- Low capacitance
- Low leakage current
- Low clamping voltage
- Flammability Rating: UL 94V-0

Pin Diagram



MARKING

3324P

PACKAGE INFORMATION

Package	MPQ	Leader Size
DFN2510	3K	7 inch

ORDER INFORMATION

Part Number	Type
KS3V3ULK4-C	Lead (Pb)-free and Halogen-free

ABSOLUTE MAXIMUM RATINGS (T_A=25℃ unless otherwise specified)

Parameter		Symbol	Value	Unit
IEC 61000-4-2 ESD Voltage	Air Contact	V_{ESD}	±25	kV
	Contact Discharge		±20	
Peak Pulse Power (tp=8/20us)		P_{PP}	56	W
Peak Pulse Current		I_{PP}	4	A
Maximum Lead Solder Temperature (10 Second Duration)		T_L	260	℃
Operating Junction Temperature Range		T_J	-55~125	
Storage Temperature Range		T_{STG}	-55~150	

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reverse Stand-off Voltage	V_{RWM}	-	-	3.3	V	Any I/O pin to GND
Breakdown Voltage	$V_{(BR)}$	4.2	-	-	V	I_T=1mA, Any I/O pin to GND
Clamping Voltage @tp=8/20μs	V_C	-	-	10	V	I_{PP}=1A, Any I/O pin to GND
		-	-	14		I_{PP}=4A, Any I/O pin to GND
Reverse Leakage Current	I_R	-	-	1	μA	V_{RWM}=3.3V, Any I/O pin to GND
Parasitic Capacitance	C_{ESD}	-	0.4	-	pF	V_R=0V, f=1MHz, Between I/O and GND
		-	0.2	-		V_R=0V, f=1MHz, Between I/O and I/O

Note:
1. I/O pins are pin 1,2,4,5, GND pins are pin 3,8.

TYPICAL CHARACTERISTICS

Fig 1 Power Derating Curve

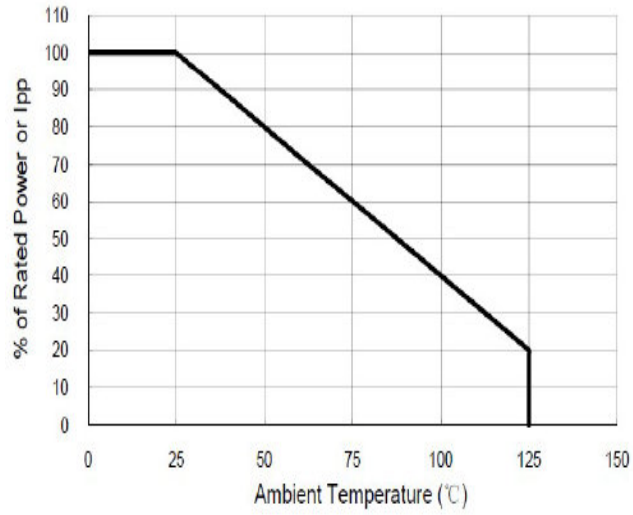


Fig 2 Clamping Voltage vs Peak Pulse Current

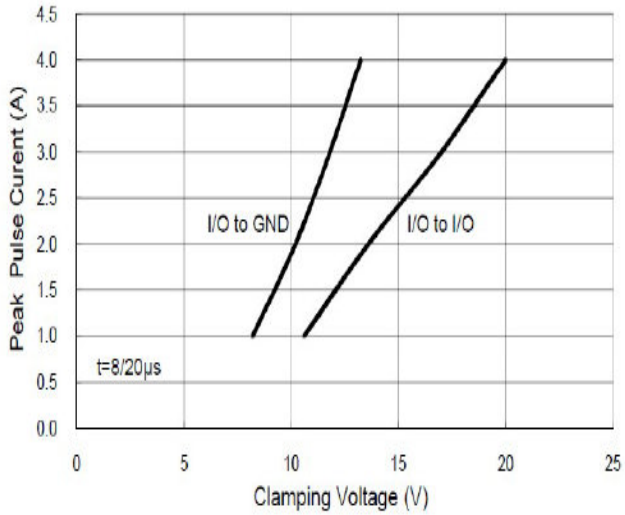


Fig 3 Voltage Sweeping of I/O to I/O

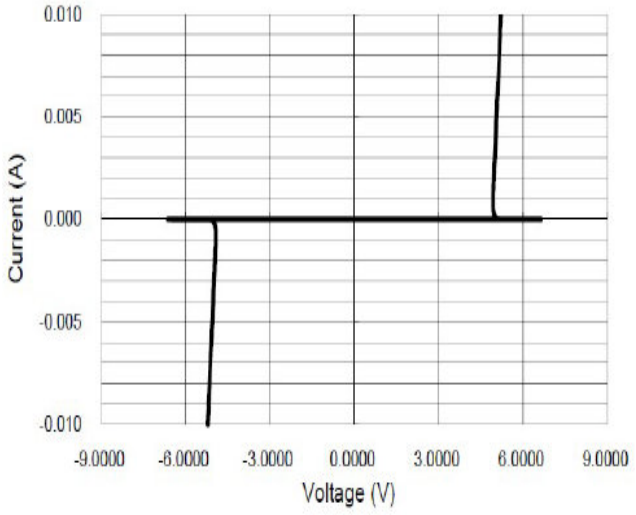
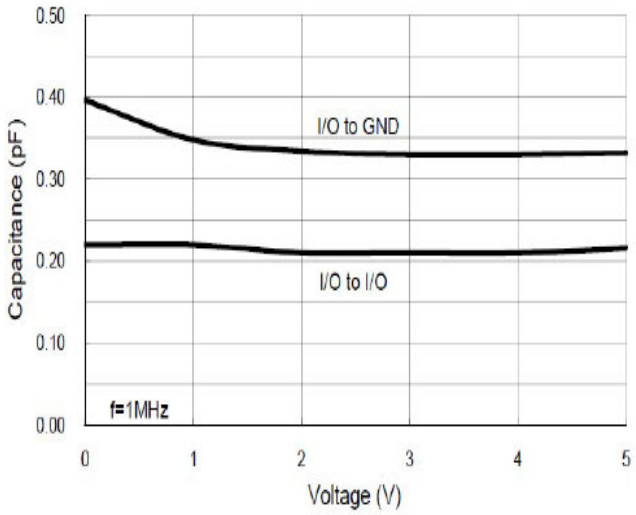


Fig 4 Voltage vs Capacitance



TYPICAL CHARACTERISTICS

Fig 5 ESD Clamping of I/O to GND
(+8kV Contact per IEC 61000-4-2)

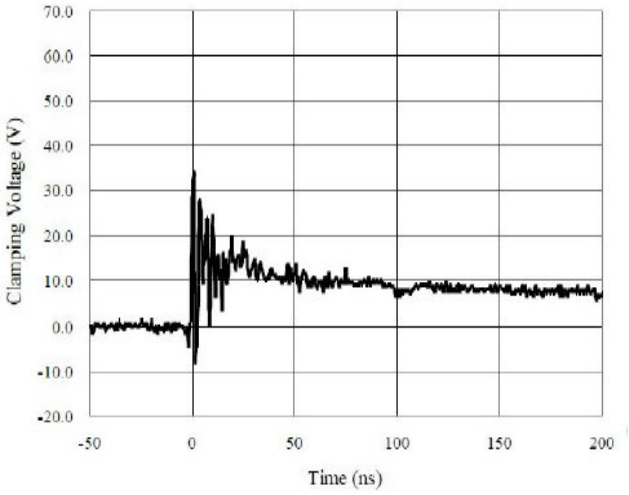


Fig 6 ESD Clamping of I/O to GND
(-8kV Contact per IEC 61000-4-2)

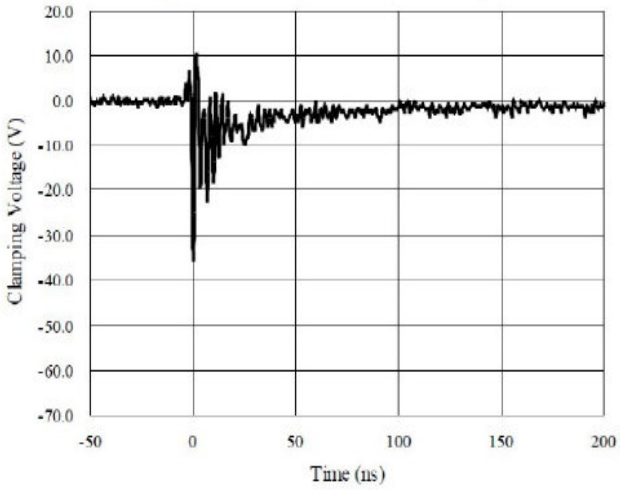
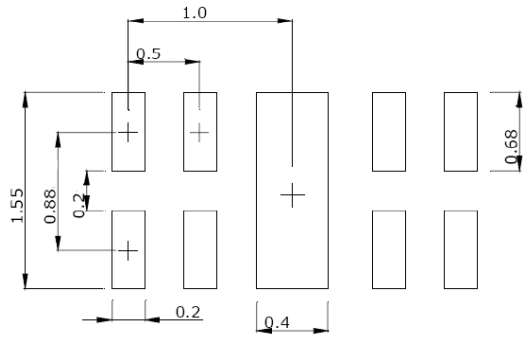


Fig 7 Mounting Pad Layout



*Dimensions in millimeters