Elektronische Bauelemente

SDT3585S-C

N & P-Ch Enhancement Mode MOSFET

N-Ch: 5A, 20V, $R_{DS(ON)}$ 37mΩ

P-Ch: -3.5A, -20V, $R_{DS(ON)}$ 75mΩ

RoHS Compliant Product
A suffix of "-C" specifies halogen and lead-free

DESCRIPTION

The SDT3585S-C is the highest performance trench N+P MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The SDT3585S-C meet the RoHS and Green Product requirement with full function reliability approved.

APPLICATIONS

- Power Management In Note Book
- Portable Equipment
- DC/DC Converter
- Load Switch

MARKING

3585S
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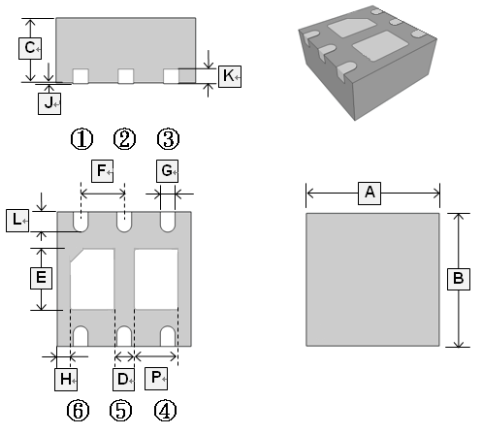
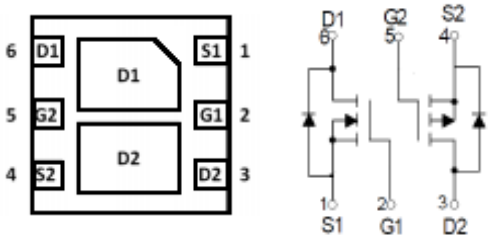
DFN2x2-6L-J



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	1.90	2.10	G	0.25	0.35
B	1.90	2.10	H	0.20 BSC.	
C	0.675	0.80	J	-	0.06
D	0.25	0.35	K	0.15	0.25
E	0.75	1.10	L	0.20	0.38
F	0.65 TYP.		P	0.52	0.72



PACKAGE INFORMATION

Package	MPQ	Leader Size
DFN2×2-6L-J	3K	7 inch

ORDER INFORMATION

Part Number	Type
SDT3585S-C	Lead (Pb)-free and Halogen-free

ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise specified)

Parameter		Symbol	Rating		Unit
			N-ch	P-ch	
Drain-Source Voltage		V_{DS}	20	-20	V
Gate-Source Voltage		V_{GS}	±12	±12	V
Continuous Drain Current [1] @V_{GS}=4.5V	T_A=25°C	I_D	5	-3.5	A
	T_A=70°C		4	-2.8	
Pulsed Drain Current [3]		I_{DM}	17	-12	A
Total Power Dissipation	T_A=25°C	P_D	1.5		W
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55~150		°C
Thermal Data					
Maximum Thermal Resistance from Junction-Ambient [1]		$R_{\theta JA}$	t≦ 5sec, 83		°C/W
			Steady State, 125		
Maximum Thermal Resistance from Junction-Ambient [2]			250		
Maximum Thermal Resistance from Junction-Case [1]		$R_{\theta JC}$	8.4		

N-CH ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain-Source Breakdown Voltage	BV_{DSS}	20	-	-	V	V_{GS}=0, I_D=250μA
Breakdown Voltage Temperature Coefficient	$\triangle BV_{DSS}/\triangle T_J$	-	0.018	-	V/°C	Reference to 25°C, I_D=1mA
Gate-Threshold Voltage	$V_{GS(th)}$	0.5	-	1.2	V	V_{DS}=V_{GS}, I_D=250μA
Forward Transfer conductance	g_{fs}	-	20	-	S	V_{DS}=5V, I_D=4A
Gate-Body Leakage Current	I_{GSS}	-	-	±100	nA	V_{DS}=0,V_{GS}= ±12V
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1	μA	V_{DS}=16V, V_{GS}=0,T_J=25°C
		-	-	5		V_{DS}=16V, V_{GS}=0,T_J=55°C
Drain-Source On-Resistance [4]	$R_{DS(ON)}$	-	-	37	mΩ	V_{GS}=4.5V, I_D=4A
		-	-	45		V_{GS}=2.5V, I_D=3A
Total Gate Charge	Q_g	-	8.6	-	nC	V_{DS}=15V V_{GS}=4.5V I_D=4A
Gate-Source Charge	Q_{gs}	-	1.37	-		
Gate-Drain Charge	Q_{gd}	-	2.3	-		
Turn-On Delay Time	$T_{d(on)}$	-	5.2	-	nS	V_{DS}=10V V_{GS}=4.5V I_D=4A R_G=3.3Ω R_D=2.5Ω
Rise Time	T_r	-	34	-		
Turn-Off Delay Time	$T_{d(off)}$	-	23	-		
Fall Time	T_f	-	9.2	-		
Input Capacitance	C_{iss}	-	635	-	pF	V_{DS}=15V V_{GS}=0 f=1MHz
Output Capacitance	C_{oss}	-	70	-		
Reverse Transfer Capacitance	C_{rss}	-	63	-		
Source-Drain Diode						
Continuous Source Current [1]	I_S	-	-	5	A	
Pulsed Source Current [3]	I_{SM}	-	-	17	A	
Forward On Voltage [4]	V_{SD}	-	0.7	1.2	V	I_S=1A, V_{GS}=0V
Reverse Recovery Time	T_{rr}	-	7.5	-	nS	I_S=4A,V_{GS}=0V, dI/dt=100A/μs
Reverse Recovery Charge	Q_{rr}	-	2.1	-	nC	

Notes:
1. Surface mounted on a 1 inch^2 FR-4 board with 2oz copper.
2. Surface mounted on FR-4 Board using the minimum recommended pad size.
3. Pulse width limited by maximum junction temperature.
4. The data tested by pulsed, pulse width≦300μs, duty cycle≦2%.

P-CH ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain-Source Breakdown Voltage	BV_{DSS}	-20	-	-	V	V_{GS}=0, I_D= -250μA
Breakdown Voltage Temperature Coefficient	$\triangle BV_{DSS}/\triangle T_J$	-	-0.01	-	V/°C	Reference to 25°C, I_D= -1mA
Gate-Threshold Voltage	$V_{GS(th)}$	-0.5	-	-1.2	V	V_{DS}=V_{GS}, I_D= -250μA
Forward Transfer conductance	g_{fs}	-	9	-	S	V_{DS}= -5V, I_D= -3A
Gate-Body Leakage Current	I_{GSS}	-	-	±100	nA	V_{DS}=0, V_{GS}= ±12V
Zero Gate Voltage Drain Current	I_{DSS}	-	-	-1	μA	V_{DS}= -16V, V_{GS}=0, T_J=25°C
		-	-	-5		V_{DS}= -16V, V_{GS}=0, T_J=55°C
Drain-Source On-Resistance [4]	$R_{DS(ON)}$	-	-	75	mΩ	V_{GS}= -4.5V, I_D= -3A
		-	-	105		V_{GS}= -2.5V, I_D= -2A
Total Gate Charge	Q_g	-	9.7	-	nC	V_{DS}= -15V V_{GS}= -4.5V I_D= -3A
Gate-Source Charge	Q_{gs}	-	2.05	-		
Gate-Drain Charge	Q_{gd}	-	2.43	-		
Turn-On Delay Time	$T_{d(on)}$	-	4.8	-	nS	V_{DS}= -10V V_{GS}= -4.5V I_D= -3A R_G=3.3Ω R_D=3.33Ω
Rise Time	T_r	-	9.6	-		
Turn-Off Delay Time	$T_{d(off)}$	-	52	-		
Fall Time	T_f	-	8.4	-		
Input Capacitance	C_{iss}	-	686	-	pF	V_{DS}= -15V V_{GS}=0 f=1MHz
Output Capacitance	C_{oss}	-	90.8	-		
Reverse Transfer Capacitance	C_{rss}	-	80.4	-		
Source-Drain Diode						
Continuous Source Current[1]	I_S			-3.5	A	
Pulsed Source Current[3]	I_{SM}			-12	A	
Forward On Voltage[4]	V_{SD}		-0.7	-1.2	V	I_S= -1A, V_{GS}=0V
Reverse Recovery Time	T_{rr}	-	8.4	-	nS	I_S= -3A, V_{GS}=0V, dI/dt=100A/μs
Reverse Recovery Charge	Q_{rr}	-	3.3	-	nC	

Notes:
1. Surface mounted on a 1 inch^2 FR-4 board with 2oz copper.
2. Surface mounted on FR-4 Board using the minimum recommended pad size.
3. Pulse width limited by maximum junction temperature.
4. The data tested by pulsed, pulse width≦300μs, duty cycle≦2%.

N-CH CHARACTERISTIC CURVE

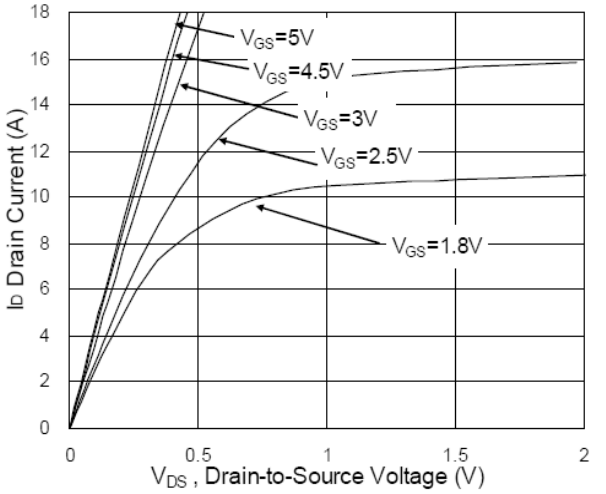


Fig.1 Typical Output Characteristics

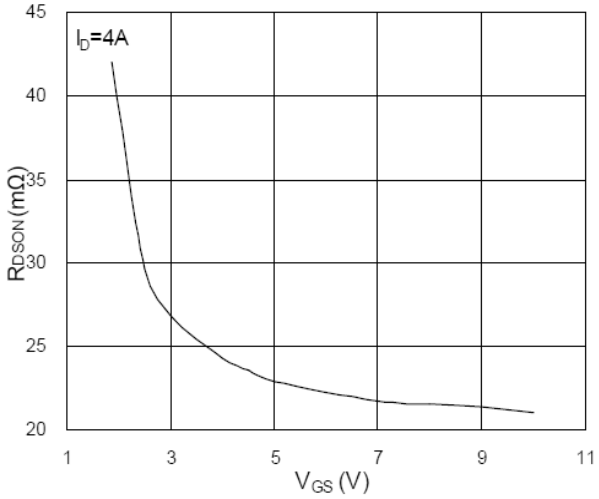


Fig.2 On-Resistance vs. Gate-Source

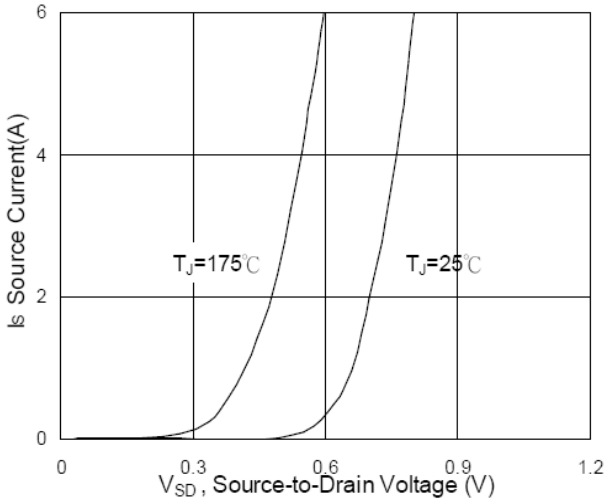


Fig.3 Forward Characteristics Of Reverse

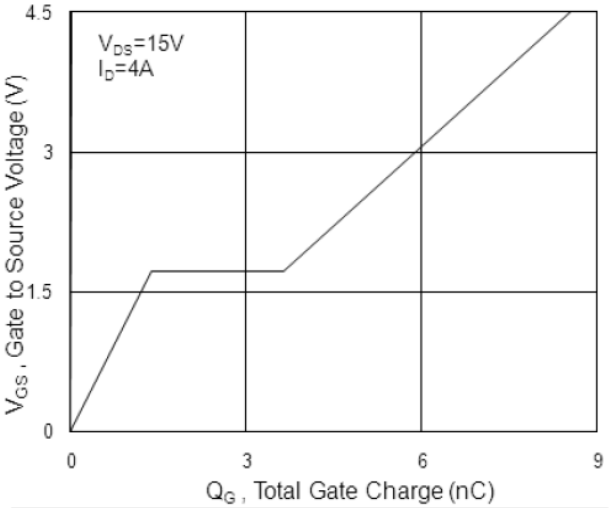


Fig.4 Gate-Charge Characteristics

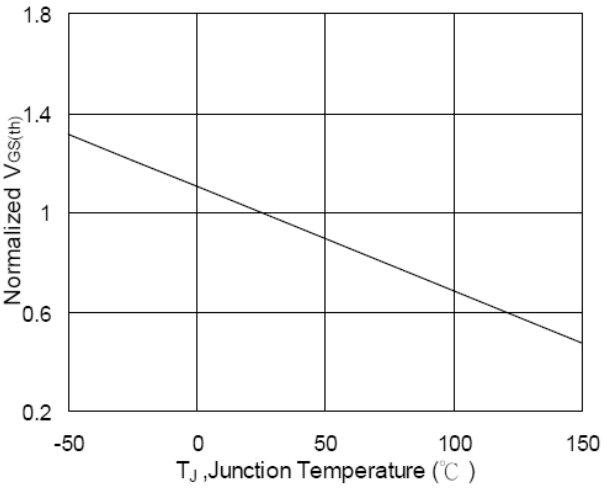


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

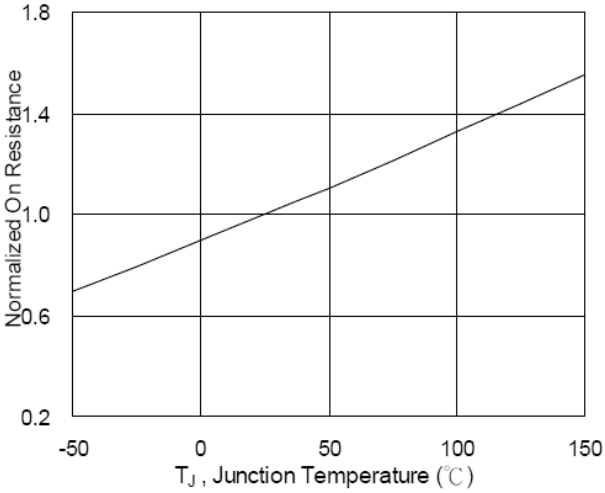


Fig.6 Normalized R_{DSON} vs. T_J

N-CH CHARACTERISTIC CURVE

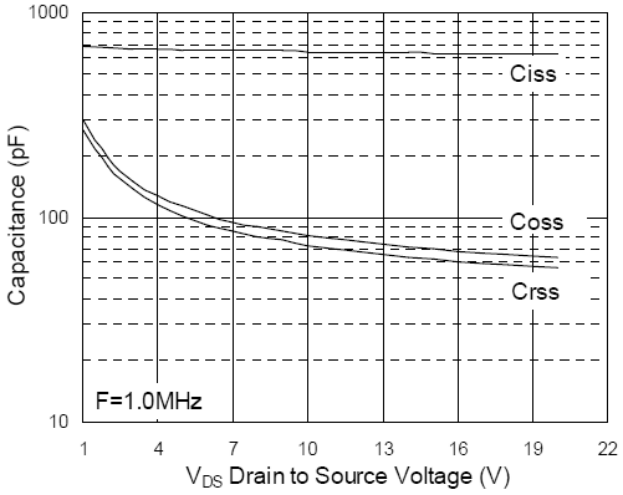


Fig.7 Capacitance

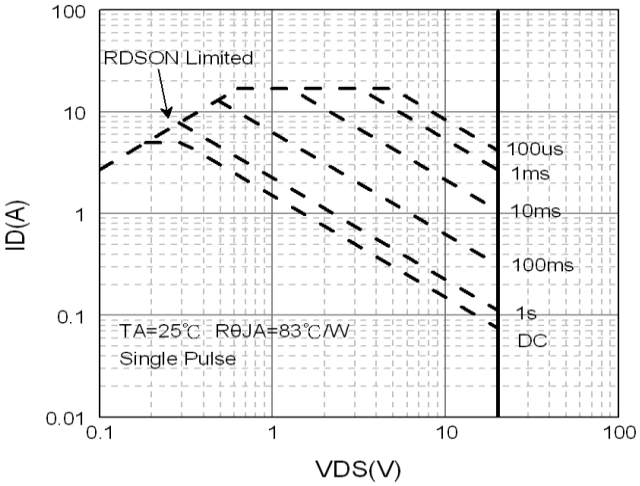


Fig.8 Safe Operating Area

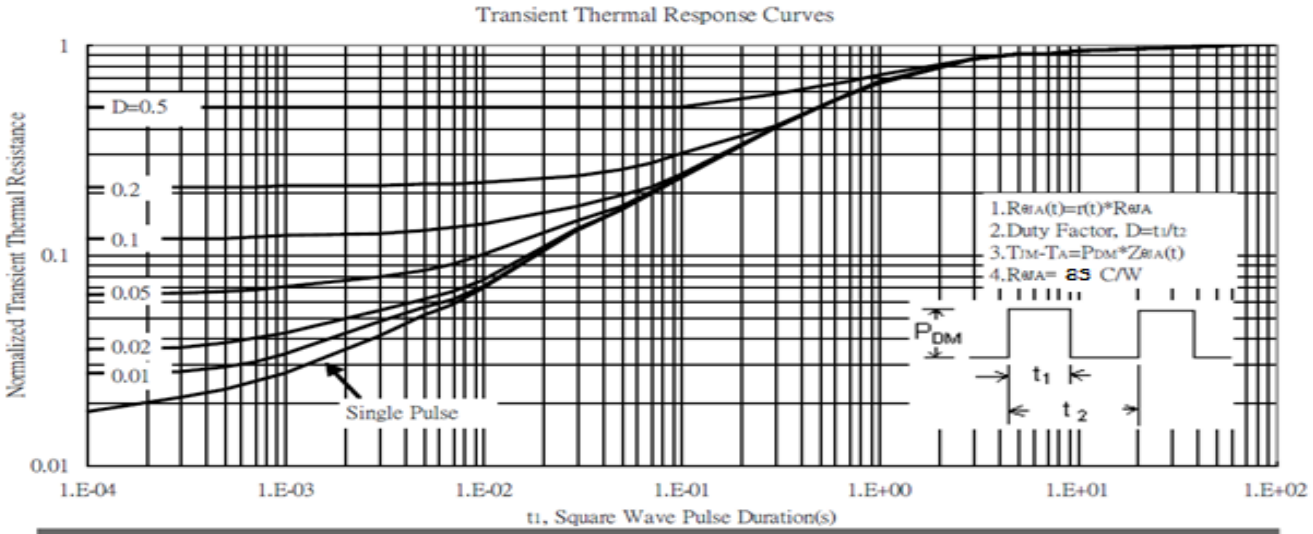


Fig.9 Normalized Maximum Transient Thermal Impedance

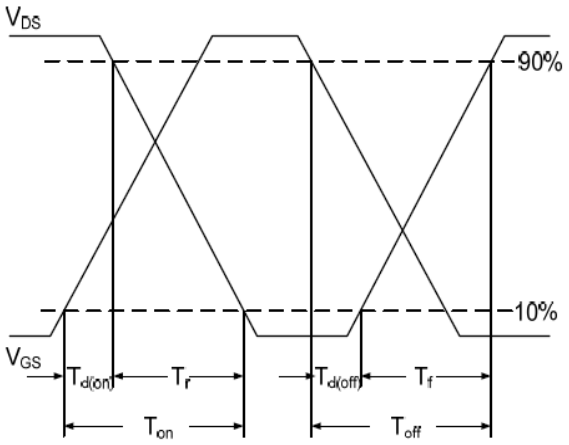


Fig.10 Switching Time Waveform

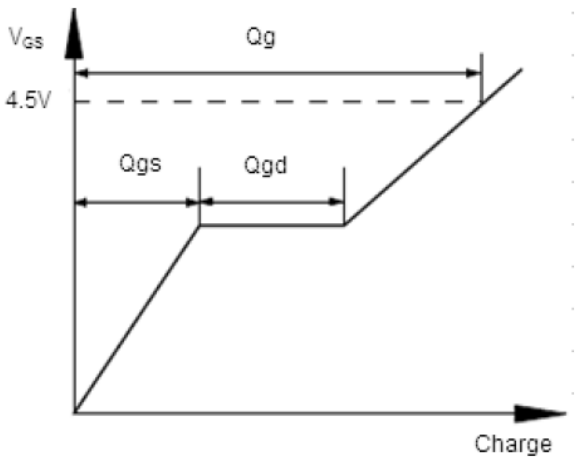
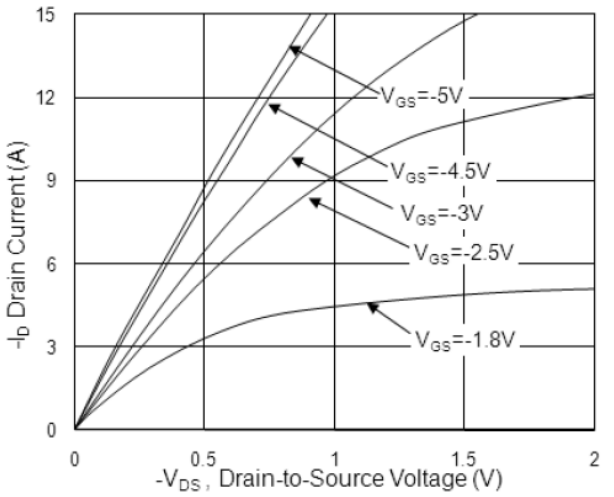


Fig.11 Gate Charge Waveform

P-CH CHARACTERISTIC CURVE



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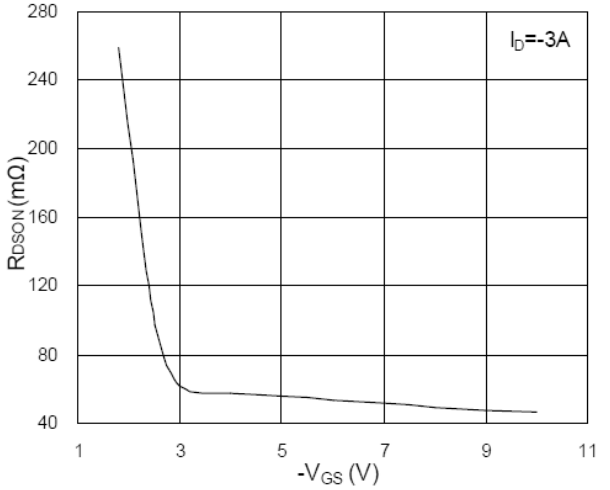

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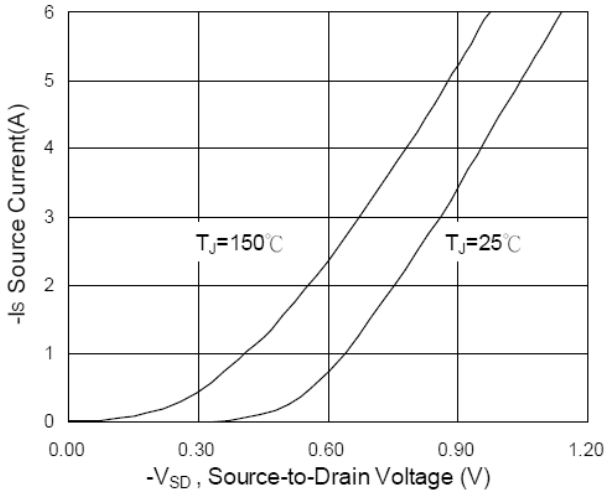

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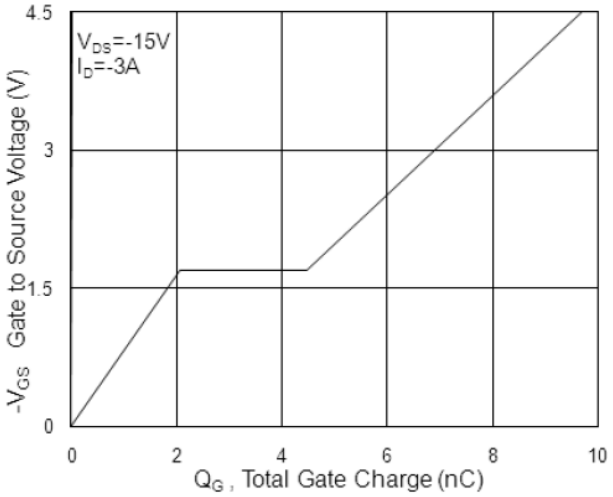


Fig.4 Gate-Charge Characteristics

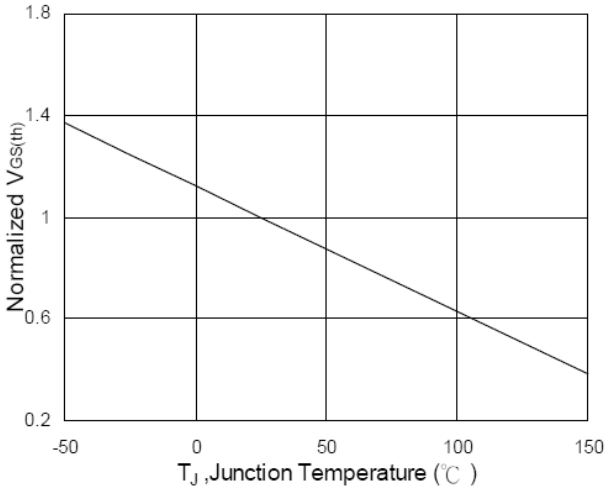


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

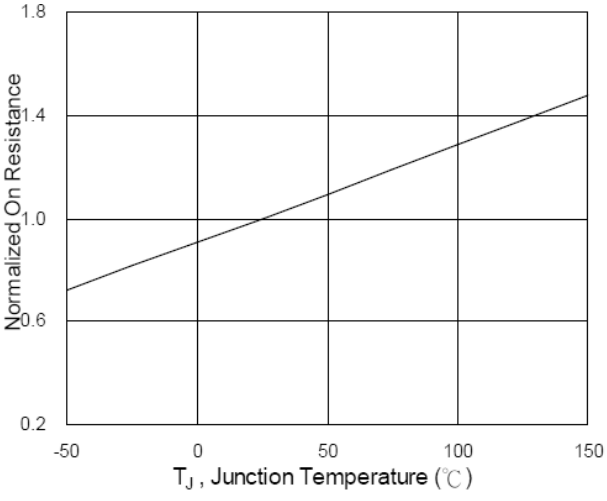


Fig.6 Normalized R_{DSON} vs. T_J

P-CH CHARACTERISTIC CURVE

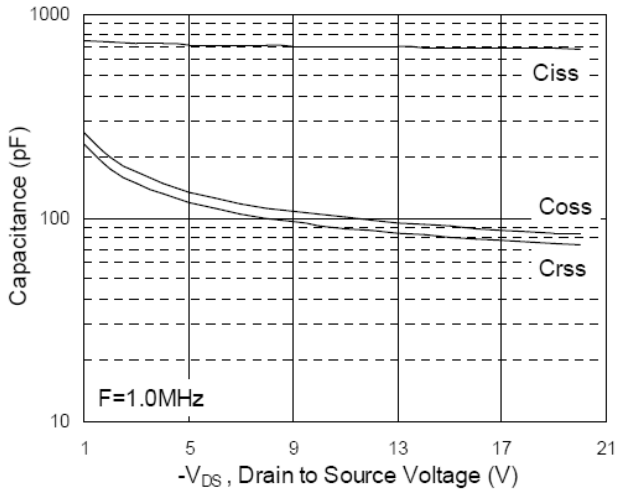
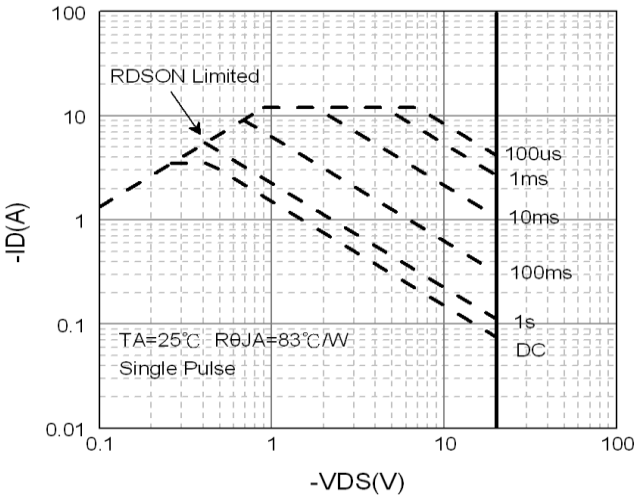


Fig.7 Capacitance



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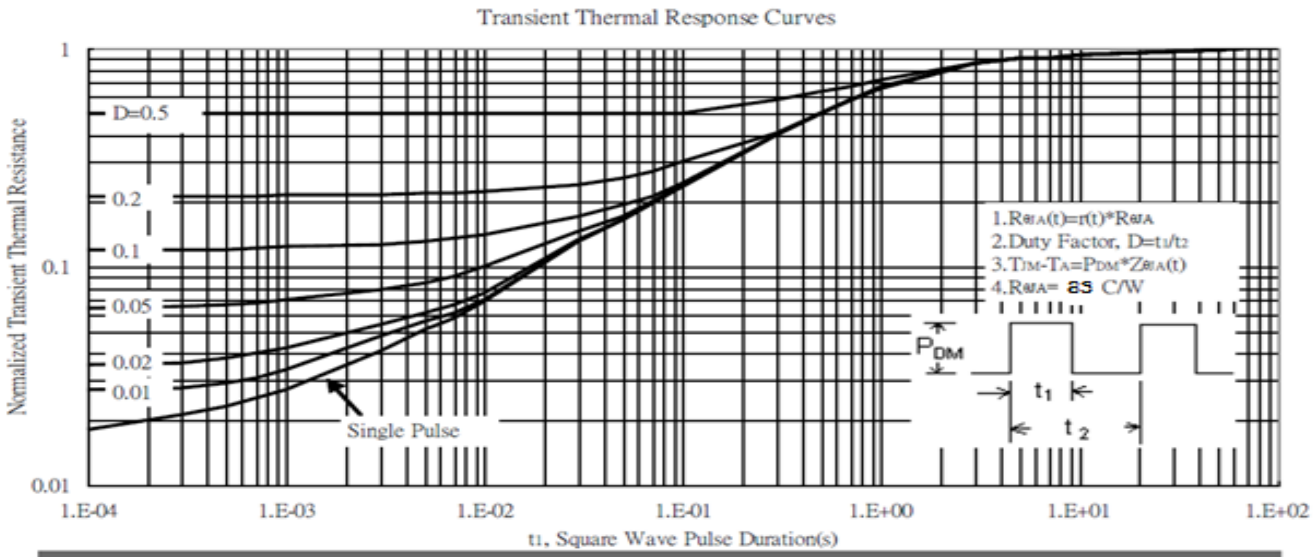

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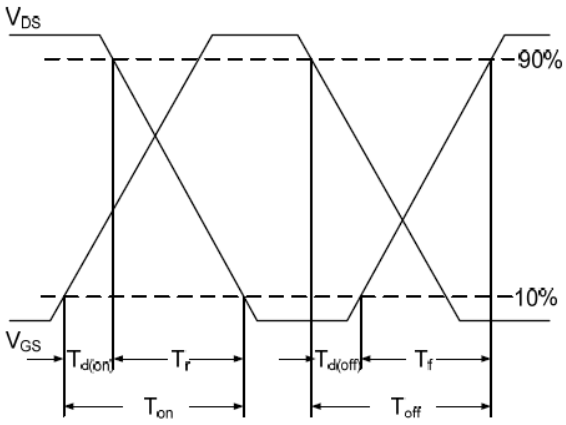


Fig.10 Switching Time Waveform

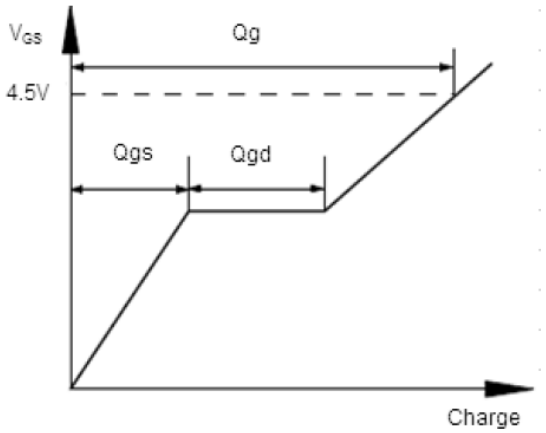
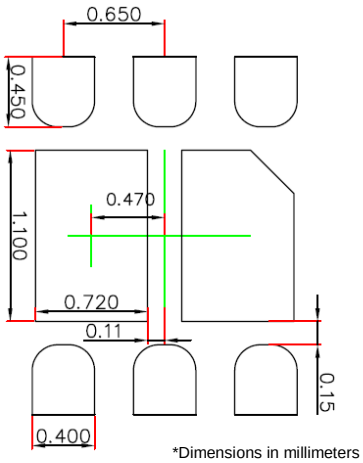


Fig.11 Gate Charge Waveform

CHARACTERISTIC CURVE



*Dimensions in millimeters

Fig.13 Mounting Pad Layout