

RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

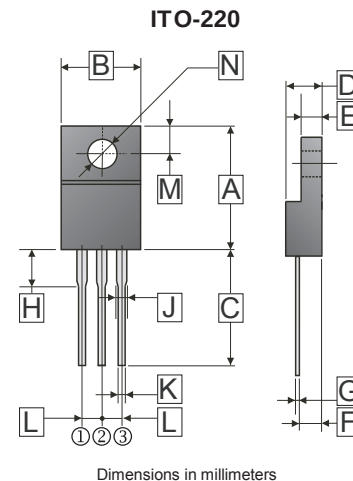
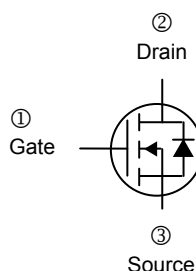
These miniature surface mount MOSFETs utilize a high cell density trench process to provide Low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Low thermal impedance copper leadframe ITO-220 saves board space.
- Fast switching speed.
- High performance trench technology.

PRODUCT SUMMARY

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$V_{DS}(V)$	$R_{DS(on)}$ m(Ω)	$I_D(A)$
100	78@ $V_{GS}=10V$	51 ^a
	92@ $V_{GS}=4.5V$	



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	15.00	15.60	H	3.00	3.80
B	9.50	10.50	J	0.90	1.50
C	13.00 Min		K	0.50	0.90
D	4.30	4.70	L	2.34	2.74
E	2.50	3.10	M	2.50	2.90
F	2.40	2.80	N	ϕ 3.1	ϕ 3.4
G	0.30	0.70			

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^a	$I_D @ T_C=25^\circ C$	51	A
Pulsed Drain Current ^b	I_{DM}	240	A
Continuous Source Current (Diode Conduction) ^a	I_S	90	A
Total Power Dissipation ^a	$P_D @ T_C=25^\circ C$	300	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ 175	$^\circ C$
THERMAL RESISTANCE RATINGS			
Maximum Thermal Resistance Junction-Ambient ^a	$R_{\theta JA}$	62.5	$^\circ C / W$
Maximum Thermal Resistance Junction-Case	$R_{\theta JC}$	0.5	$^\circ C / W$

Notes :

- a. Package Limited.
b. Pulse width limited by maximum junction temperature.

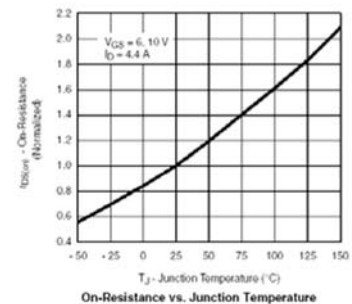
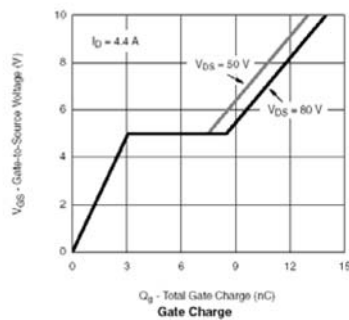
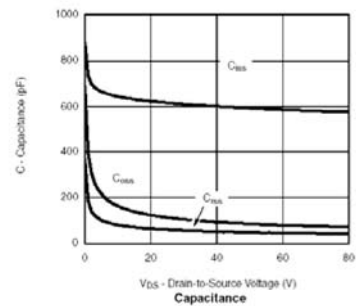
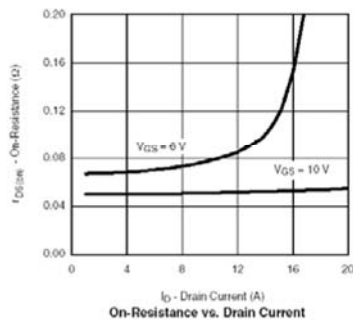
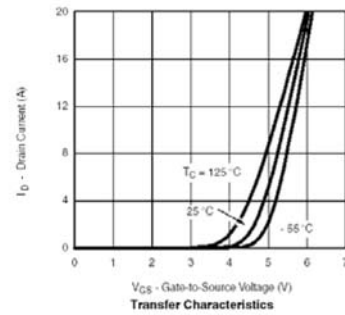
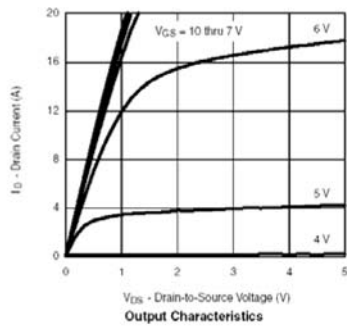
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ C$ unless otherwise specified)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	1	-	-	V	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$
Gate-Body Leakage	I_{GSS}	-	-	± 100	nA	$V_{DS} = 0V$, $V_{GS} = 20V$
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1	μA	$V_{DS} = 80V$, $V_{GS} = 0V$
		-	-	25		$V_{DS} = 80V$, $V_{GS} = 0V$, $T_J = 55^\circ C$
On-State Drain Current ^a	$I_{D(on)}$	120	-	-	A	$V_{DS} = 5V$, $V_{GS} = 10V$
Drain-Source On-Resistance ^a	$R_{DS(ON)}$	-	-	78	m Ω	$V_{GS} = 10V$, $I_D = 30 A$
		-	-	92		$V_{GS} = 4.5V$, $I_D = 20 A$
Forward Transconductance ^a	g_{fs}	-	30	-	S	$V_{DS} = 15V$, $I_D = 30 A$
Diode Forward Voltage	V_{SD}	-	1.1	-	V	$I_S = 34 A$, $V_{GS} = 0 V$
Dynamic ^b						
Total Gate Charge	Q_g	-	8.5	-	nC	$V_{DS} = 15 V$ $V_{GS} = 4.5 V$ $I_D = 90 A$
Gate-Source Charge	Q_{gs}	-	3.3	-		
Gate-Drain Charge	Q_{gd}	-	4.0	-		
Turn-on Delay Time	$T_{d(on)}$	-	18	-	nS	$V_{DD} = 25 V$ $I_D = 34 A$ $V_{GEN} = 10 V$ $R_L = 25 \Omega$
Rise Time	T_r	-	59	-		
Turn-off Delay Time	$T_{d(off)}$	-	37	-		
Fall Time	T_f	-	9	-		

Notes

- a. Pulse test : Pulse width $\leq 300 \mu s$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

CHARACTERISTIC CURVE



CHARACTERISTIC CURVE

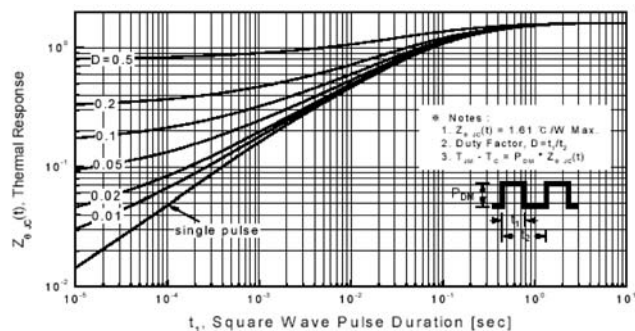
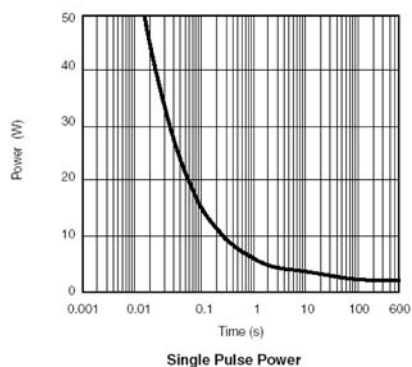
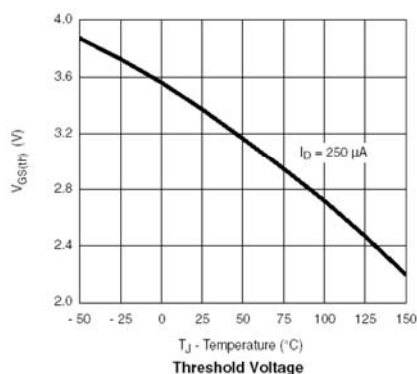
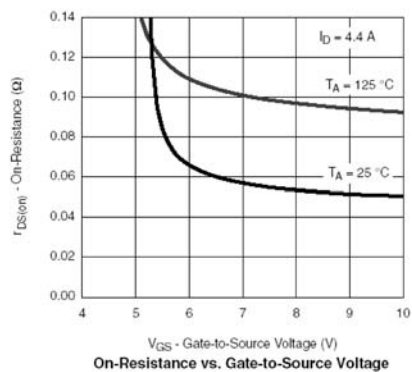
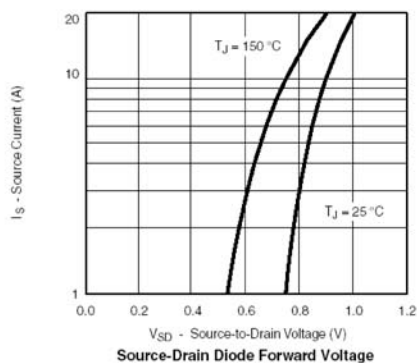


Figure 11. Transient Thermal Response Curve