Elektronische Bauelemente

SPR100N08SV-C

100A, 80V, $R_{DS(ON)}$ 3mΩ

N-Channel Shielded Gate Trench Power MOSFET

RoHS Compliant Product

A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

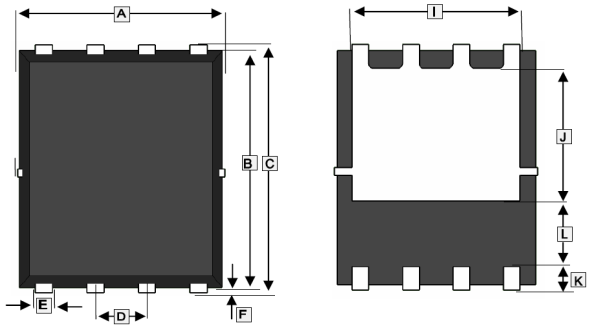
The SPR100N08SV-C is the Shielded Gate Technology N-ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The SPR100N08SV-C meet the RoHS and Green Product requirement with full function reliability approved.

FEATURES

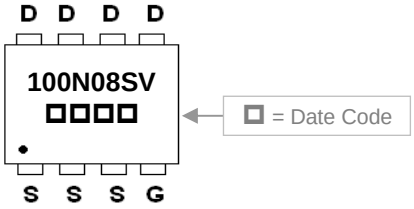
- Shielded Gate Trench Technology
- Super Low Gate Charge
- Green Device Available

PR-8PP



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.90	5.10	G	0.80	1.10
B	5.70	5.90	H	0.254 REF.	
C	5.90	6.20	I	4.00 REF.	
D	1.27 BSC.		J	3.40 REF.	
E	0.33	0.51	K	0.60 REF.	
F	0.06	0.20	L	1.40 REF.	

MARKING

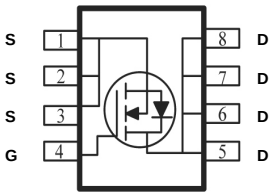


PACKAGE INFORMATION

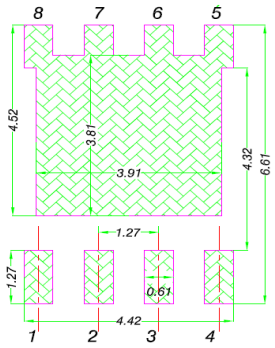
Package	MPQ	Leader Size
PR-8PP	3K	13 inch

ORDER INFORMATION

Part Number	Type
SPR100N08SV-C	Lead (Pb)-free and Halogen-free



Mounting Pad Layout



*Dimensions in millimeters

ABSOLUTE MAXIMUM RATINGS (T_J=25℃ unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	80	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1,5] @V_{GS}=10V	T_C=25℃	I_D	100	A
	T_C=100℃		99	
Pulsed Drain Current [2]		I_{DM}	250	A
Power Dissipation [3]	T_C=25℃	P_D	125	W
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55~150	℃
Thermal Resistance Ratings				
Thermal Resistance Junction-Ambient [1]		$R_{\theta JA}$	55	℃/W
Thermal Resistance Junction-Case [1]		$R_{\theta JC}$	1	

ELECTRICAL CHARACTERISTICS (T_J=25℃ unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	80	-	-	V	V_{GS}=0V, I_D=250μA
Gate-Threshold Voltage		$V_{GS(th)}$	2	-	4	V	V_{DS}=V_{GS}, I_D=250μA
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}=±20V, V_{DS}=0V
Drain-Source Leakage Current	T_J=25℃	I_{DSS}	-	-	1	uA	V_{DS}=64V, V_{GS}=0V
	T_J=55℃		-	-	5		
Static Drain-Source On-Resistance [2]		$R_{DS(ON)}$	-	2.3	3	mΩ	V_{GS}=10V, I_D=20A
Gate Resistance		R_g	-	1.4	-	Ω	f=1MHz
Total Gate Charge		Q_g	-	104	-	nC	I_D=20A V_{DS}=64V V_{GS}=10V
Gate-Source Charge		Q_{gs}	-	23.8	-		
Gate-Drain Change		Q_{gd}	-	28.9	-		
Turn-on Delay Time		$T_{d(on)}$	-	22	-	nS	V_{DD}=40V I_D=20A V_{GS}=10V R_G=3Ω
Rise Time		T_r	-	16	-		
Turn-off Delay Time		$T_{d(off)}$	-	54	-		
Fall Time		T_f	-	16	-		
Input Capacitance		C_{iss}	-	6286	-	pF	V_{GS}=0V V_{DS}=40V f=1MHz
Output Capacitance		C_{oss}	-	1108	-		
Reverse Transfer Capacitance		C_{rss}	-	50	-		
Source-Drain Diode							
Diode Forward Voltage [2]		V_{SD}	-	-	1.2	V	I_S=1A, V_{GS}=0V, T_J=25℃
Continuous Source Current [1,5]		I_S	-	-	100	A	V_G=V_D=0V, Force Current

Notes:

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2oz copper.
2. The data tested by pulsed, pulse width≤300us, duty cycle≤2%.
3. The power dissipation is limited by 150℃ juncti on temperature.
4. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.
5. Package limitation current is 100A.

CHARACTERISTIC CURVES

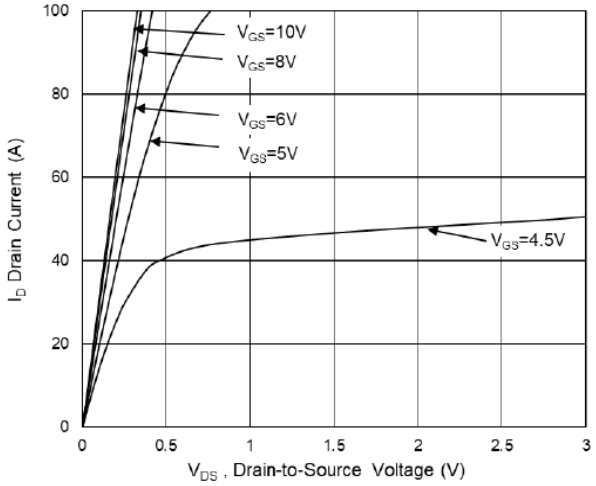


Fig.1 Typical Output Characteristics

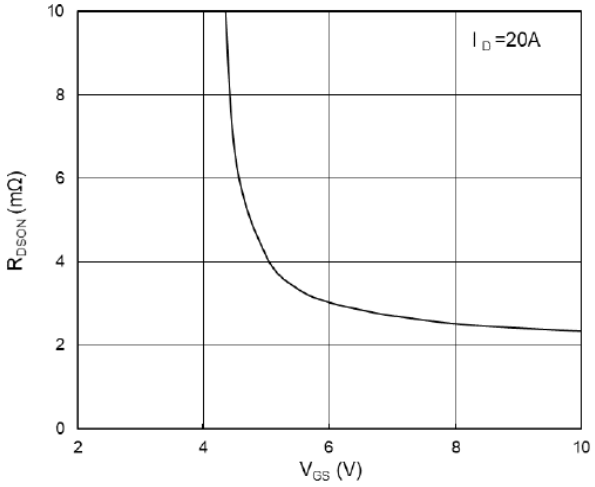


Fig.2 On-Resistance vs G-S Voltage

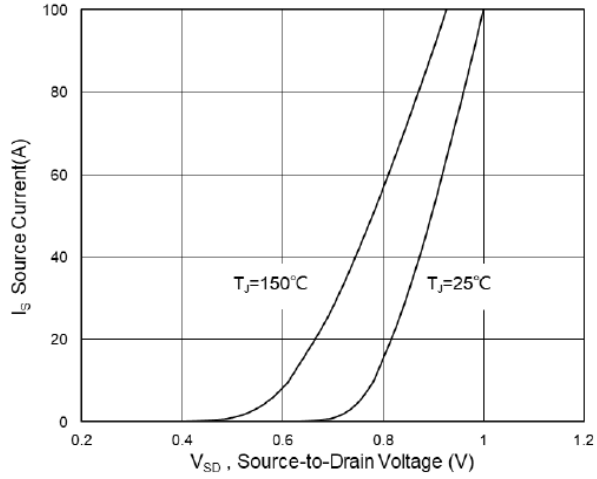


Fig.3 Source Drain Forward Characteristics

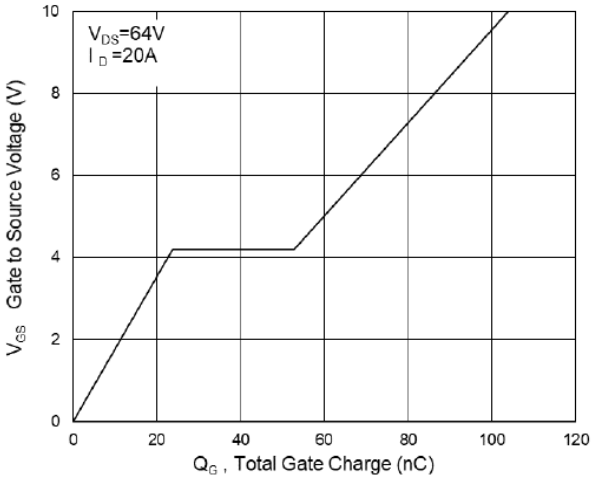


Fig.4 Gate-Charge Characteristics

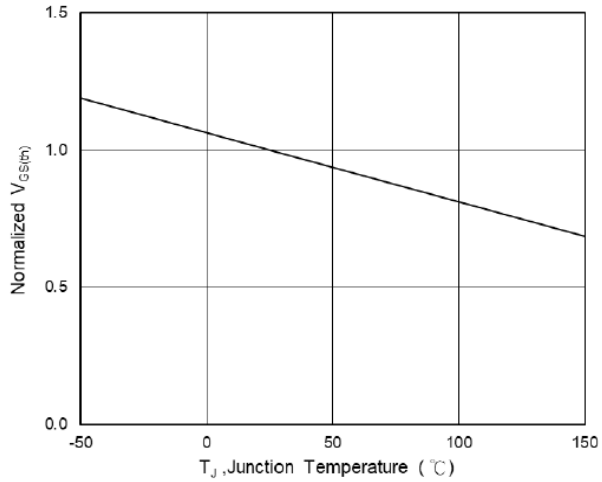


Fig.5 Normalized $V_{GS(th)}$ vs T_J

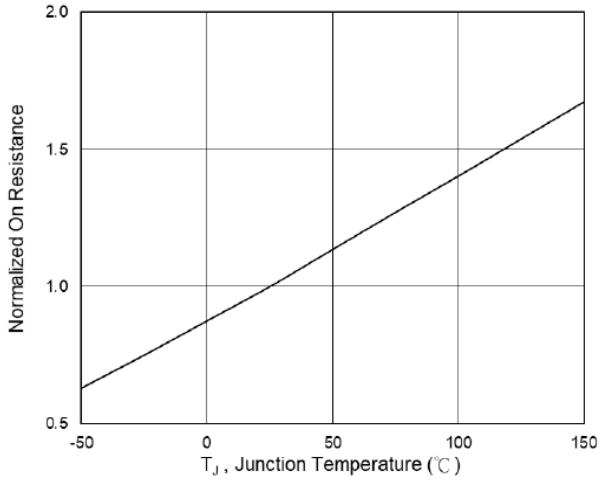


Fig.6 Normalized R_{DSON} vs T_J

CHARACTERISTIC CURVES

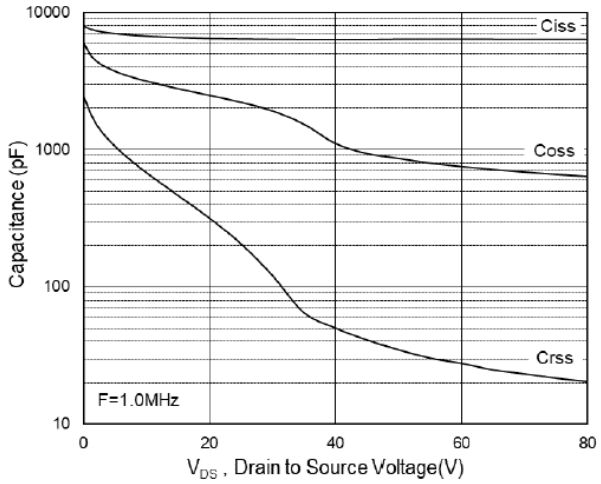


Fig.7 Capacitance

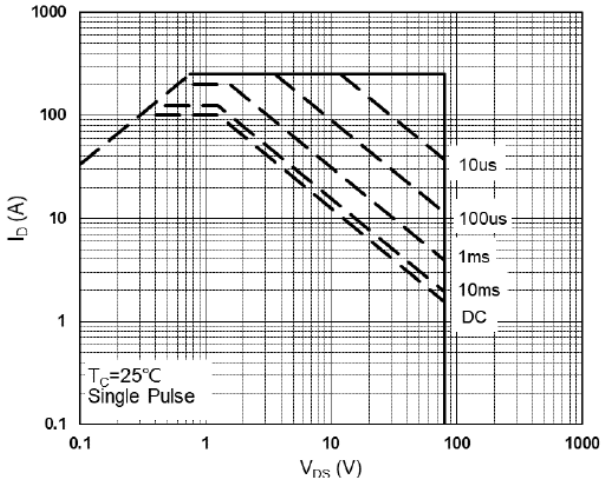


Fig.8 Safe Operating Area

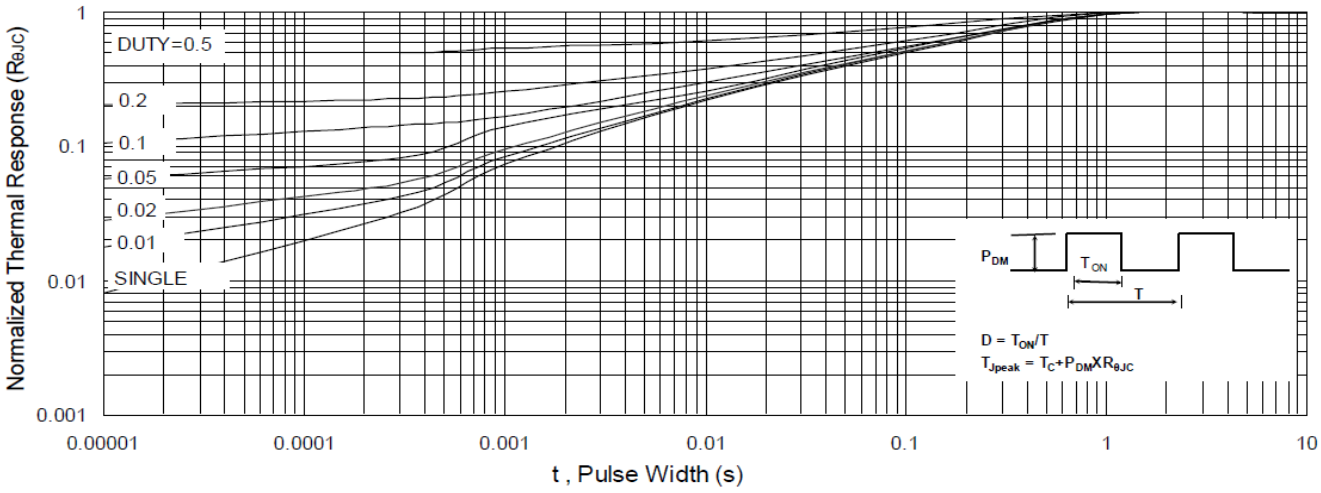


Fig.9 Normalized Maximum Transient Thermal Impedance

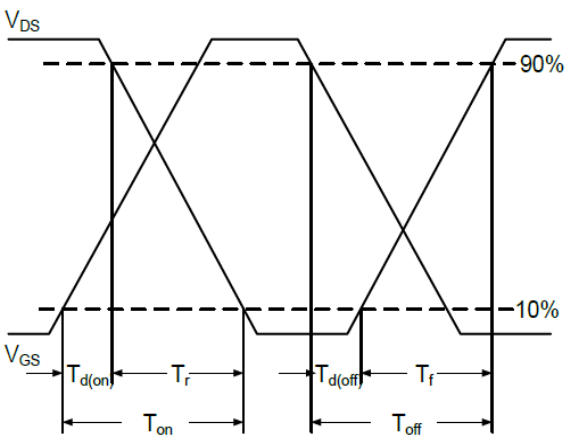


Fig.10 Switching Time Waveform

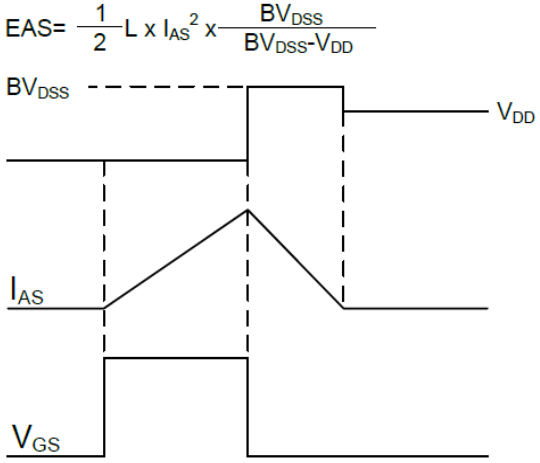


Fig.11 Unclamped Inductive Switching Waveform