Elektronische Bauelemente

SPR50N03-C

51A, 30V, $R_{DS(ON)}$ 9mΩ

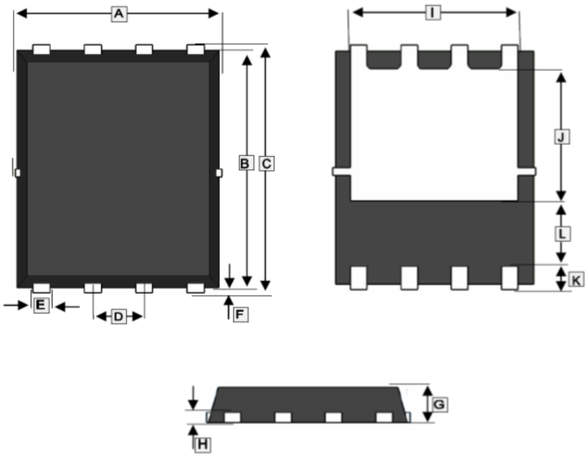
N-Channel Enhancement Mode Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

The SPR50N03-C provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness. The PR-8PP package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

PR-8PP

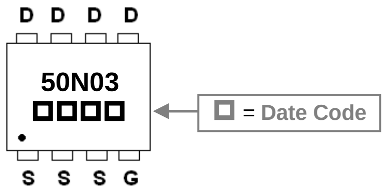


REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.90	5.10	G	0.80	1.00
B	5.70	5.90	H	0.254 REF.	
C	5.95	6.20	I	4.00 REF.	
D	1.27 BSC.		J	3.40 REF.	
E	0.35	0.49	K	0.60 REF.	
F	0.10	0.20	L	1.40 REF.	

FEATURES

- Lower Gate Charge
- Simple Drive Requirement
- Fast Switching Characteristic

MARKING

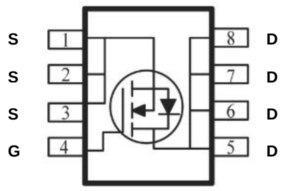


PACKAGE INFORMATION

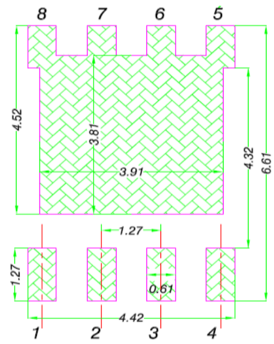
Package	MPQ	Leader Size
PR-8PP	3K	13 inch

ORDER INFORMATION

Part Number	Type
SPR50N03-C	Lead (Pb)-free and Halogen-free



Mounting Pad Layout



*Dimensions in millimeters

ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise specified)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [1] @V_{GS}=10V	T_C=25°C	I_D	51	A
	T_C=100°C		36	
	T_A=25°C		12	
	T_A=70°C		9.6	
Pulsed Drain Current [2]		I_{DM}	130	A
Single Pulse Avalanche Energy [3]		E_{AS}	57.8	mJ
Avalanche Current		I_{AS}	34	A
Power Dissipation [4]	T_C=25°C	P_D	46	W
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55~150	°C
Thermal Resistance Rating				
Maximum Thermal Resistance Junction-Ambient [1]		$R_{θJA}$	62	°C/W
Maximum Thermal Resistance Junction-Case [1]		$R_{θJC}$	2.7	

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Drain-Source Breakdown Voltage		BV_{DSS}	30	-	-	V	V_{GS}=0, I_D=250uA
Gate-Threshold Voltage		$V_{GS(th)}$	1	-	2.5	V	V_{DS}=V_{GS}, I_D=250uA
Forward Tranconductance		g_{fs}	-	42	-	S	V_{DS}=5V, I_D=30A
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current	T_J=25°C	I_{DSS}	-	-	1	uA	V_{DS}=24V, V_{GS}=0
	T_J=55°C		-	-	5		
Static Drain-Source On-Resistance [2]		$R_{DS(ON)}$	-	-	9	mΩ	V_{GS}=10V, I_D=30A
			-	-	13.5		V_{GS}=4.5V, I_D=15A
Gate Resistance		R_g	-	2.1	3.5	Ω	f=1MHz
Total Gate Charge		Q_g	-	10.6	-	nC	I_D=15A V_{DS}=15V V_{GS}=4.5V
Gate-Source Charge		Q_{gs}	-	4.2	-		
Gate-Drain ("Miller") Change		Q_{gd}	-	4	-		
Turn-on Delay Time [2]		$T_{d(on)}$	-	6.4	-	nS	V_{DD}=15V I_D=15A V_{GS}=10V R_G=3.3Ω
Rise Time		T_r	-	70.6	-		
Turn-off Delay Time		$T_{d(off)}$	-	22.4	-		
Fall Time		T_f	-	8	-		
Input Capacitance		C_{iss}	-	1127	-	pF	V_{GS}=0 V_{DS}=15V f=1MHz
Output Capacitance		C_{oss}	-	194	-		
Reverse Transfer Capacitance		C_{rss}	-	77	-		
Single Pulse Avalanche Energy [5]		E_{AS}	20	-	-	mJ	V_{DD}=25V, L=0.1mH, I_{AS}=20A
Source-Drain Diode							
Diode Forward Voltage [2]		V_{SD}	-	-	1	V	I_S=1A, V_{GS}=0V
Continuous Source Current [1 6]		I_S	-	-	51	A	V_G=V_D=0, Force Current
Pulsed Source Current [2 6]		I_{SM}	-	-	130	A	
Reverse Recovery Time		T_{rr}	-	12	-	nS	I_F=30A, dI/dt=100A/μs, T_J=25°C
Reverse Recovery Charge		Q_{rr}	-	3.7	-	nC	

Notes:

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2oz copper, ≦ 10sec, 125°C/W at steady state.
2. The data tested by pulsed, pulse width≦ 300us, duty cycle≦ 2%.
3. The E_{AS} data shows Max. rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=34A.
4. The power dissipation is limited by 150°C junction temperature.
5. The Min. value is 100% E_{AS} tested guarantee.
6. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

CHARACTERISTIC CURVES

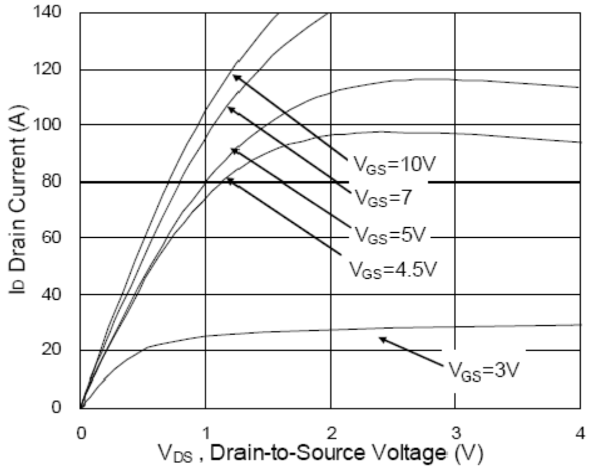


Fig.1 Typical Output Characteristics

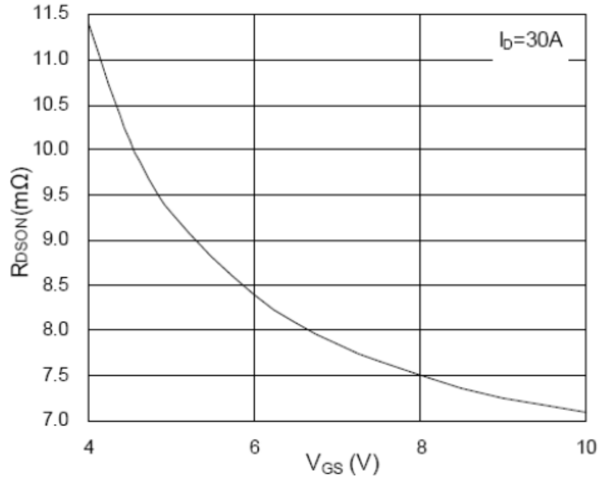


Fig.2 On-Resistance vs. Gate-Source

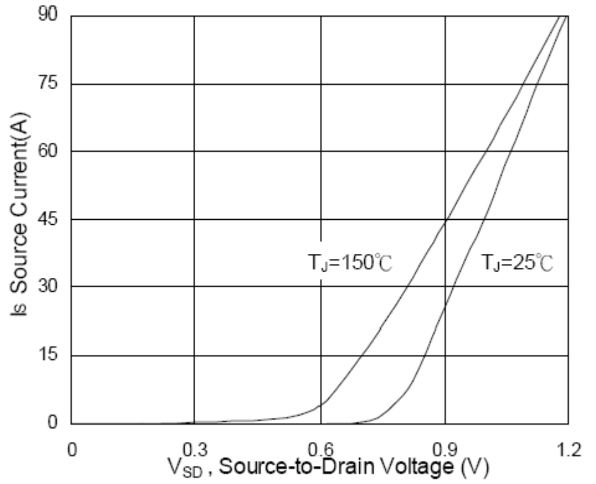


Fig.3 Forward Characteristics of Reverse

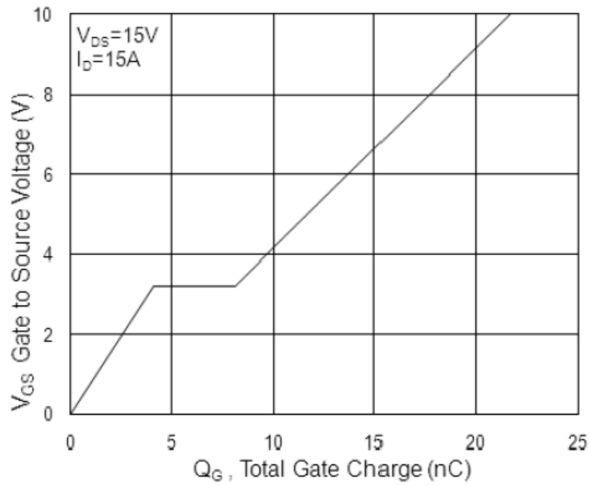


Fig.4 Gate-Charge Characteristics

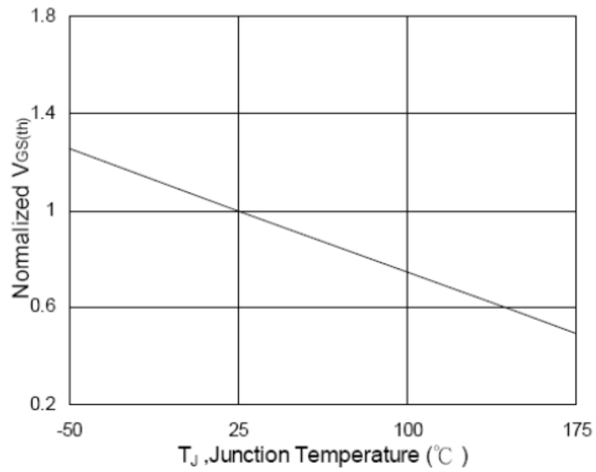


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

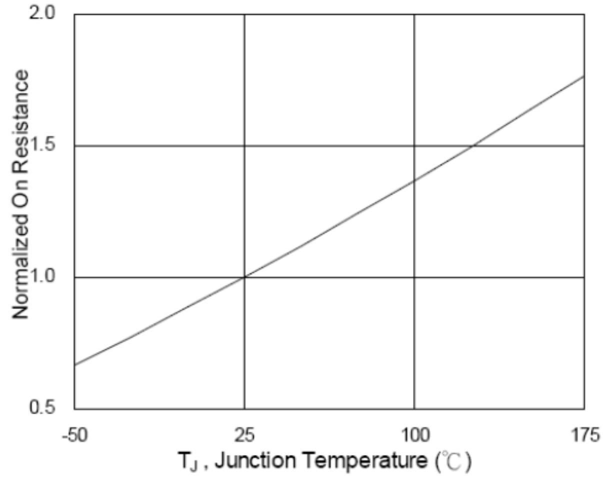


Fig.6 Normalized R_{DSON} vs. T_J

CHARACTERISTIC CURVES

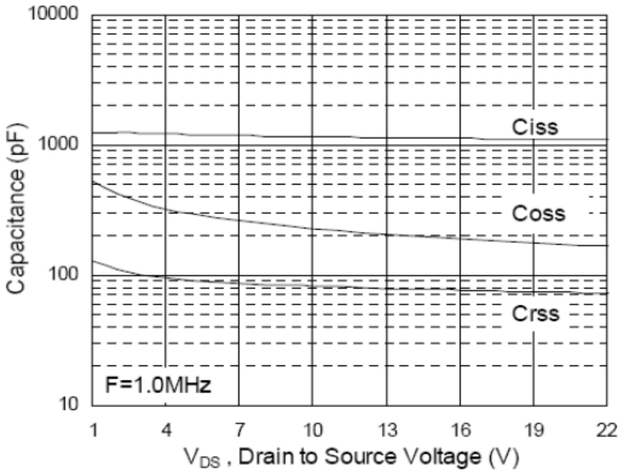


Fig.7 Capacitance

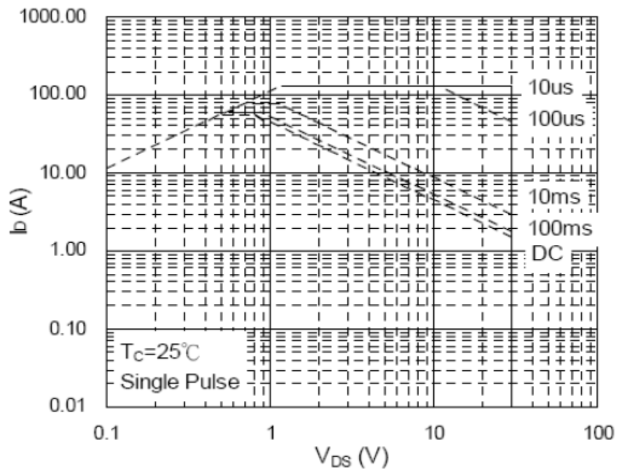


Fig.8 Safe Operating Area

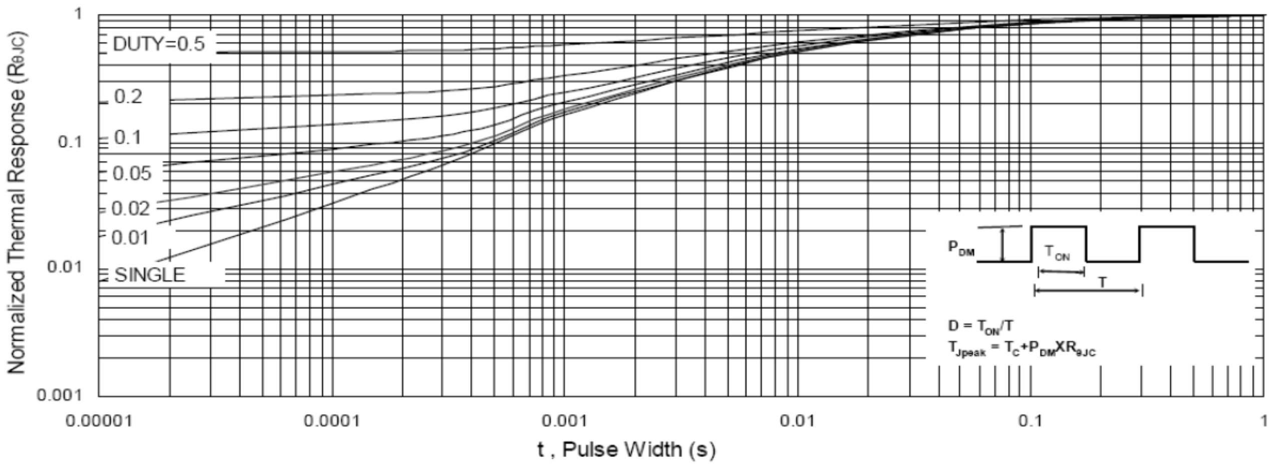


Fig.9 Normalized Maximum Transient Thermal Impedance

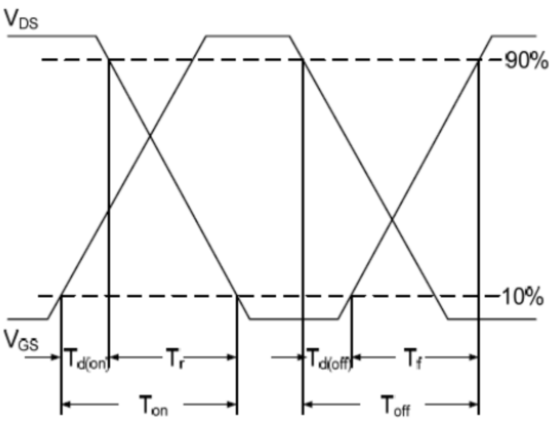


Fig.10 Switching Time Waveform

$$EAS = \frac{1}{2} L \times I_{AS}^2 \times \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

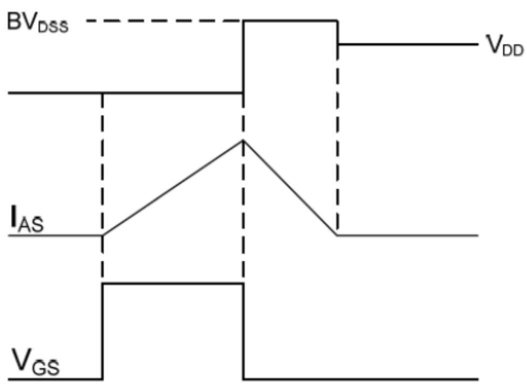


Fig.11 Unclamped Inductive Switching Waveform