

RoHS Compliant Product  
A suffix of "-C" specifies halogen & lead-free

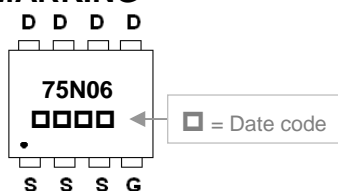
## DESCRIPTION

The SPR75N06-C provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness. The PR-8PP package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

## FEATURES

- Lower Gate Charge
- Advanced high cell density Trench technology
- Green Device Available

## MARKING



## PACKAGE INFORMATION

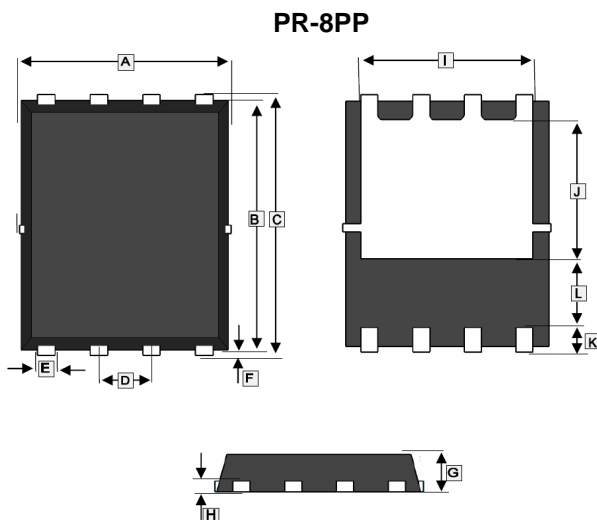
Package	MPQ	Leader Size
PR-8PP	3K	13 inch

## ORDER INFORMATION

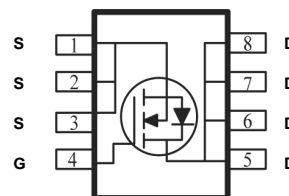
Part Number	Type
SPR75N06-C	Lead (Pb)-free and Halogen-free

## ABSOLUTE MAXIMUM RATINGS ( $T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>1</sup> @ $V_{GS}=10\text{V}$	$I_D$	$T_C=25^\circ\text{C}$	75
		$T_C=100^\circ\text{C}$	47
Pulsed Drain Current <sup>2,4</sup>	$I_{DM}$	280	A
Power Dissipation	$P_D$	89	W
Operating Junction & Storage Temperature	$T_J, T_{STG}$	-55~150	$^\circ\text{C}$
<b>Thermal Resistance Ratings</b>			
Thermal Resistance Junction-Ambient <sup>1</sup> (Max).	$R_{\theta JA}$	62	$^\circ\text{C/W}$
Thermal Resistance Junction-Case <sup>1</sup> (Max).	$R_{\theta JC}$	1.4	



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	4.9	5.1	G	0.8	1.0
B	5.7	5.9	H	0.254 Ref.	
C	5.95	6.2	I	4.0 Ref.	
D	1.27 BSC.		J	3.4 Ref.	
E	0.35	0.49	K	0.6 Ref.	
F	0.1	0.2	L	1.4 Ref.	



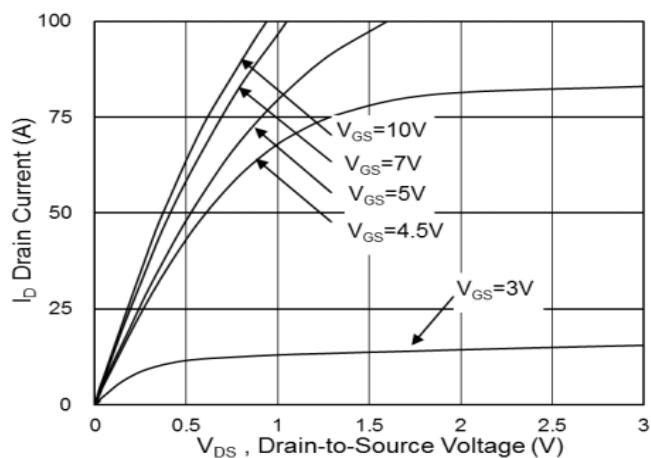
**ELECTRICAL CHARACTERISTICS** ( $T_J=25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	$BV_{DSS}$	60	-	-	V	$V_{GS}=0, I_D=250\mu\text{A}$
Gate-Threshold Voltage	$V_{GS(th)}$	1.2	-	2.5	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$
Gate-Source Leakage Current	$I_{GSS}$	-	-	$\pm 100$	nA	$V_{GS} = \pm 16\text{V}$
Drain-Source Leakage Current	$I_{DSS}$	-	-	1	uA	$V_{DS}=48\text{V}, V_{GS}=0, T_J=25^\circ\text{C}$
		-	-	5		$V_{DS}=48\text{V}, V_{GS}=0, T_J=55^\circ\text{C}$
Static Drain-Source On-Resistance <sup>3</sup>	$R_{DS(ON)}$	-	-	8.5	m $\Omega$	$V_{GS}=10\text{V}, I_D=10\text{A}$
		-	-	12		$V_{GS}=4.5\text{V}, I_D=5\text{A}$
Gate Resistance	$R_g$	-	1.2	-	$\Omega$	$V_{DS}=V_{GS}=0, f=1.0\text{MHz}$
Total Gate Charge	$Q_g$	-	57	-	nC	$I_D=18\text{A}$ $V_{DS}=30\text{V}$ $V_{GS}=10\text{V}$
Gate-Source Charge	$Q_{gs}$	-	8.7	-		
Gate-Drain Change	$Q_{gd}$	-	14	-		
Turn-on Delay Time <sup>2</sup>	$T_{d(on)}$	-	16.2	-	nS	$V_{DD}=30\text{V}$ $I_D=20\text{A}$ $V_{GS}=10\text{V}$ $R_G=3.3\Omega$
Rise Time	$T_r$	-	41.2	-		
Turn-off Delay Time	$T_{d(off)}$	-	56.4	-		
Fall Time	$T_f$	-	16.2	-		
Input Capacitance	$C_{iss}$	-	3307	-	pF	$V_{GS}=0$ $V_{DS}=30\text{V}$ $f=1.0\text{MHz}$
Output Capacitance	$C_{oss}$	-	201	-		
Reverse Transfer Capacitance	$C_{rss}$	-	151	-		
<b>Source-Drain Diode</b>						
Diode Forward Voltage <sup>3</sup>	$V_{SD}$	-	-	1.2	V	$I_S=1\text{A}, V_{GS}=0$
Continuous Source Current <sup>1</sup>	$I_S$	-	-	75	A	$V_G=V_D=0, \text{Force Current}$
Reverse Recovery Time	$T_{rr}$	-	22	-	nS	$I_F=20\text{A}, dI/dt=100\text{A}/\mu\text{s}$
Reverse Recovery Charge	$Q_{rr}$	-	72	-	nC	$T_J=25^\circ\text{C}$

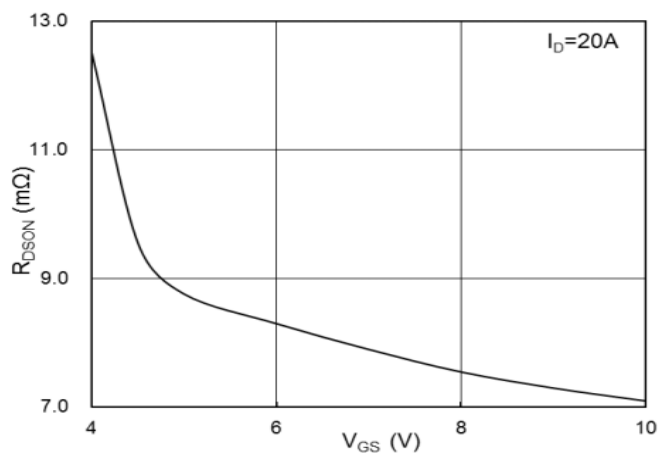
Notes:

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. The Pulse width limited by maximum junction temperature, Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$
3. The Pulse Test : Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$
4. Package limit.

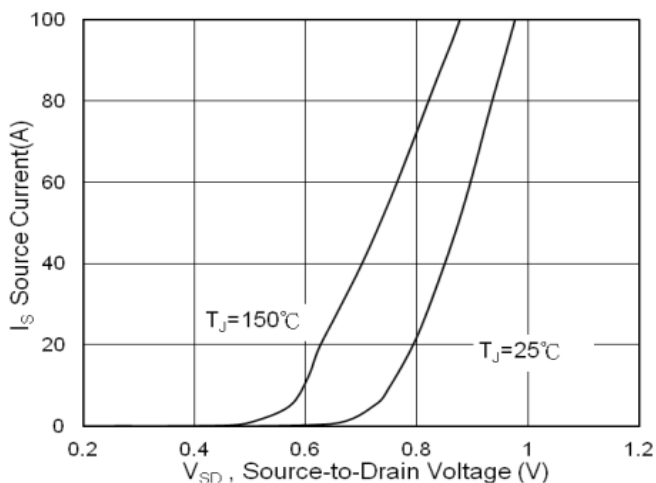
**CHARACTERISTIC CURVES**



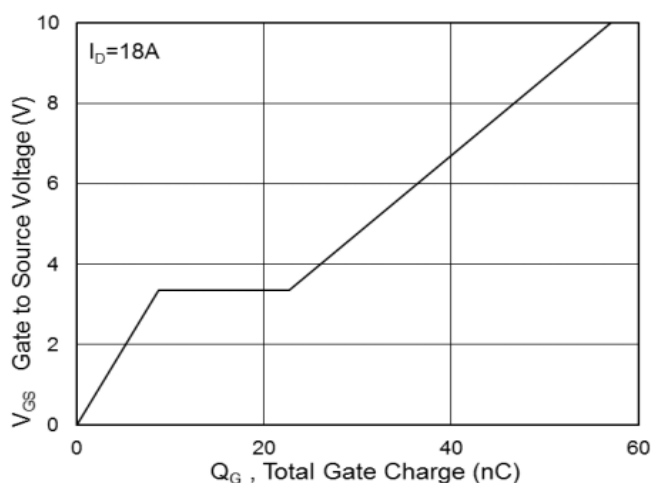
**Fig.1 Typical Output Characteristics**



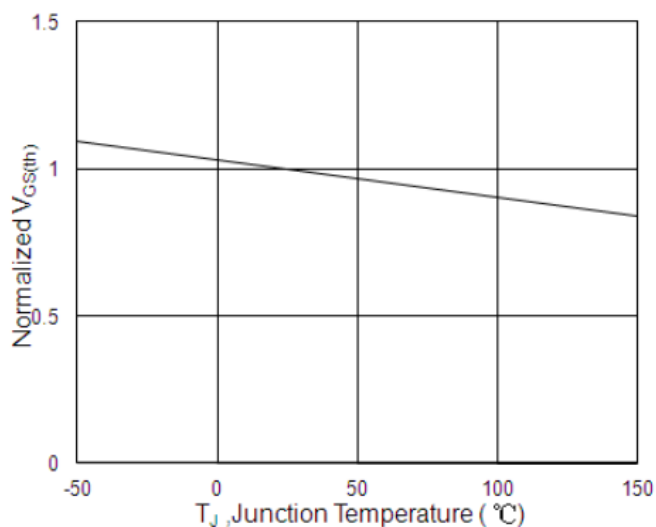
**Fig.2 On-Resistance vs Gate-Source Voltage**



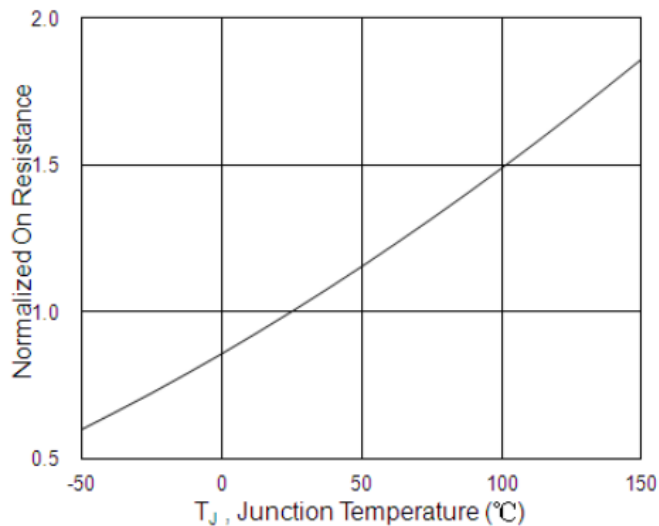
**Fig.3 Forward Characteristics of Reverse**



**Fig.4 Gate-Charge Characteristics**

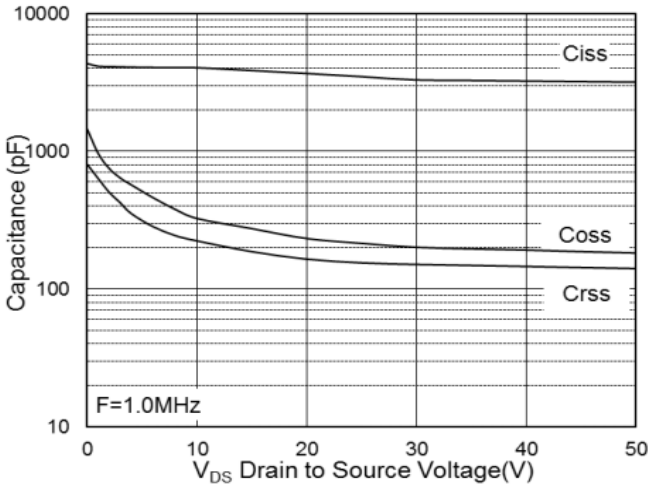


**Fig.5 Normalized  $V_{GS(th)}$  vs  $T_J$**

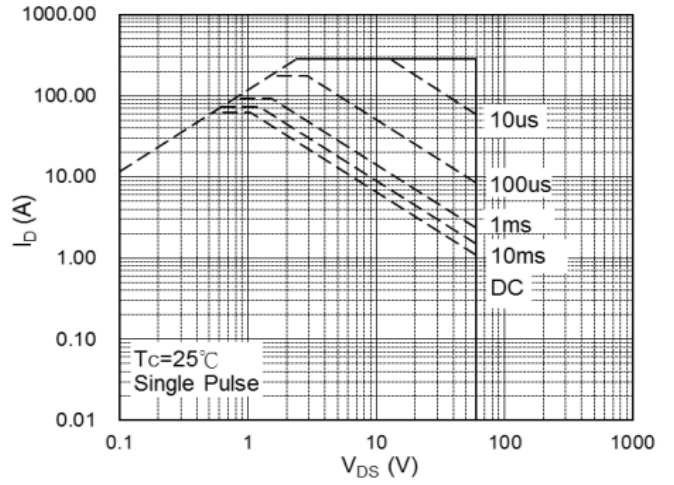


**Fig.6 Normalized  $R_{DS(ON)}$  vs  $T_J$**

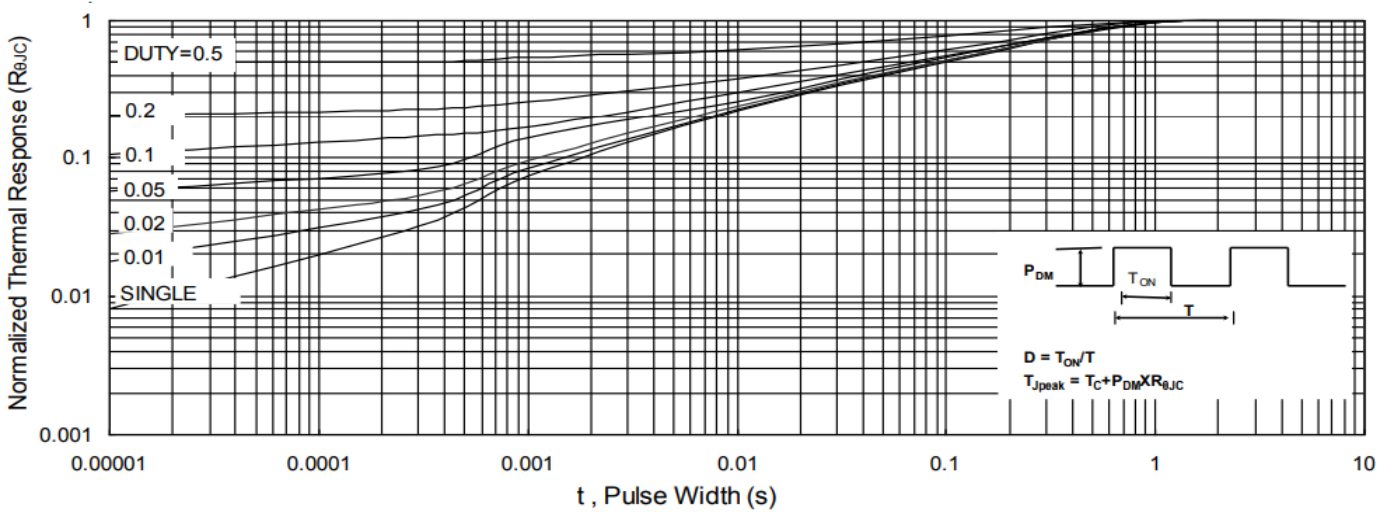
**CHARACTERISTIC CURVES**



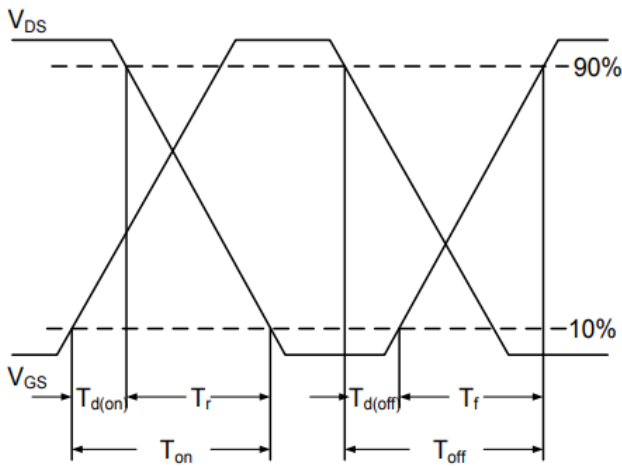
**Fig.7 Capacitance**



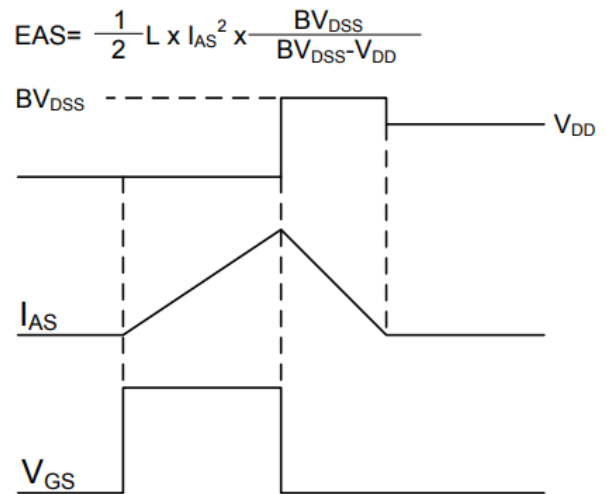
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**