

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation.

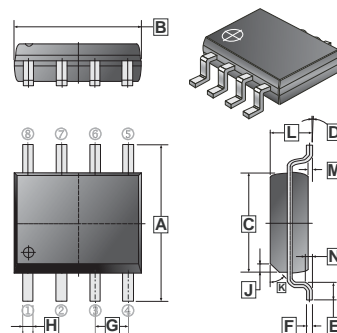
FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Low thermal impedance copper leadframe SOP-8 saves board space.
- Fast switching speed.
- High performance trench technology.

APPLICATION

DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

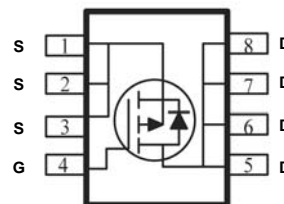
SOP-8



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.80	6.20	H	0.35	0.49
B	4.80	5.00	J	0.375 REF.	
C	3.80	4.00	K	45°	
D	0°	8°	L	1.35	1.75
E	0.40	0.90	M	0.10	0.25
F	0.19	0.25	N	0.25 REF.	
G	1.27 TYP.				

PACKAGE INFORMATION

Package	MPQ	Leader Size
SOP-8	2.5K	13' inch



MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ¹	I_D	$T_A = 25^\circ\text{C}$	-6.8
		$T_A = 70^\circ\text{C}$	-6.3
Pulsed Drain Current ²	I_{DM}	-30	A
Continuous Source Current (Diode Conduction) ¹	I_S	-2.5	A
Total Power Dissipation ¹	P_D	$T_A = 25^\circ\text{C}$	3.1
		$T_A = 70^\circ\text{C}$	2.6
Operating Junction & Storage Temperature Range	T_J, T_{STG}	-55 ~ 150	$^\circ\text{C}$
Thermal Resistance Ratings			
Thermal Resistance Junction-Ambient (Max.) ¹	$t \leq 10 \text{ sec}$	$R_{\theta JA}$	50 $^\circ\text{C} / \text{W}$

Notes:

1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	-1	-	-	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
Gate-Body Leakage Current	I_{GSS}	-	-	± 100	nA	$V_{DS}=0, V_{GS} = \pm 20\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	-	-	-1	μA	$V_{DS} = -48\text{V}, V_{GS}=0$
		-	-	-10		$V_{DS} = -48\text{V}, V_{GS}=0, T_J=55^\circ\text{C}$
On-State Drain Current ¹	$I_{D(on)}$	-20	-	-	A	$V_{DS} = -5\text{V}, V_{GS} = -10\text{V}$
Drain-Source On-Resistance ¹	$R_{DS(ON)}$	-	-	45	m Ω	$V_{GS} = -10\text{V}, I_D = -6.8\text{A}$
		-	-	60		$V_{GS} = -4.5\text{V}, I_D = -5.9\text{A}$
Forward Transconductance ¹	g_{fs}	-	8	-	S	$V_{DS} = -15\text{V}, I_D = -6.8\text{A}$
Diode Forward Voltage	V_{SD}	-	-	-1.2	V	$I_S = -2.5\text{A}, V_{GS}=0$
Dynamic ²						
Total Gate Charge	Q_g	-	18	-	nC	$I_D = -6.8\text{A}$ $V_{DS} = -30\text{V}$ $V_{GS} = -4.5\text{V}$
Gate-Source Charge	Q_{gs}	-	5	-		
Gate-Drain Charge	Q_{gd}	-	2	-		
Turn-On Delay Time	$T_{d(on)}$	-	8	-	nS	$V_{DD} = -30\text{V}$ $I_D = -1\text{A}$ $V_{GEN} = -10\text{V}$ $R_L = 30\Omega$ $R_G = 6\Omega$
Rise Time	T_r	-	10	-		
Turn-Off Delay Time	$T_{d(off)}$	-	35	-		
Fall Time	T_f	-	12	-		

Notes:

1. Pulse test : $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
2. Guaranteed by design, not subject to production testing.