

SSG4520H

N-Ch: 6.6A, 20V, $R_{DS(ON)}$ 47 m Ω
P-Ch: -5.2A, -20V, $R_{DS(ON)}$ 79 m Ω
N & P-Ch Enhancement Mode Power MOSFET

RoHS Compliant Product
 A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation.

FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Low thermal impedance copper leadframe SOP-8 saves board space
- Fast switching speed
- High performance trench technology

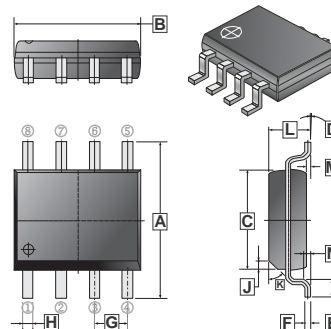
APPLICATION

DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones

PACKAGE INFORMATION

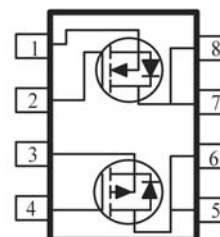
Package	MPQ	Leader Size
SOP-8	2.5K	13 inch

SOP-8



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.8	6.20	H	0.35	0.51
B	4.80	5.00	J	0.375 REF.	
C	3.80	4.00	K	45°	
D	0°	8°	L	1.35	1.75
E	0.50	0.93	M	0.10	0.25
F	0.19	0.25	N	0.25 REF.	
G	1.27 TYP.				

Top View



ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating		Unit
		N-CH	P-CH	
Drain-Source Voltage	V_{DS}	20	-20	V
Gate-Source Voltage	V_{GS}	± 8	± 8	V
Continuous Drain Current ¹	I_D	$T_A = 25^\circ\text{C}$	-5.2	A
		$T_A = 70^\circ\text{C}$	-3.8	A
Pulsed Drain Current ²	I_{DM}	20	-20	A
Continuous Source Current (Diode Conduction) ¹	I_S	2.2	-2.2	A
Total Power Dissipation ¹	P_D	$T_A = 25^\circ\text{C}$	2.1	W
		$T_A = 70^\circ\text{C}$	1.3	W
Operating Junction & Storage Temperature Range	T_J, T_{STG}	-55 ~ 150		$^\circ\text{C}$
Thermal Resistance Ratings				
Maximum Junction-to-Ambient ¹	$R_{\theta JA}$	$t \leq 10$ sec	62.5	$^\circ\text{C} / \text{W}$
		Steady State	110	$^\circ\text{C} / \text{W}$

Notes:

1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

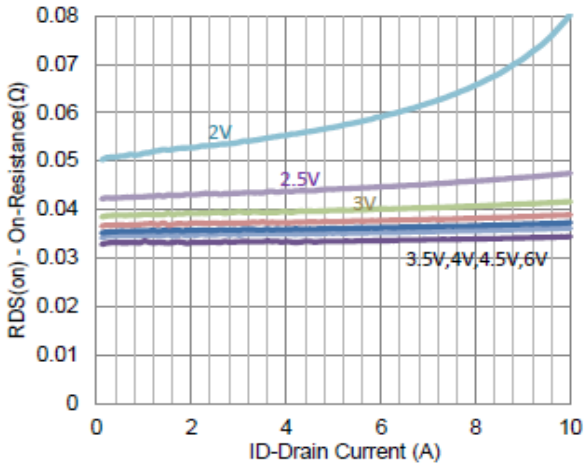
ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ch	Min.	Typ.	Max.	Unit	Teat Conditions
Static							
Gate Threshold Voltage	$V_{GS(th)}$	N	1	-	-	V	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$
		P	-1	-	-		$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$
Gate-Body Leakage	I_{GSS}	N	-	-	± 100	nA	$V_{DS}=0$, $V_{GS}=8\text{V}$
		P	-	-	± 100		$V_{DS}=0$, $V_{GS}=-8\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	N	-	-	1	μA	$V_{DS}=8\text{V}$, $V_{GS}=0$
		P	-	-	-1		$V_{DS}=-8\text{V}$, $V_{GS}=0$
On-State Drain Current ¹	$I_{D(on)}$	N	10	-	-	A	$V_{DS}=5\text{V}$, $V_{GS}=4.5\text{V}$
		P	-10	-	-		$V_{DS}=-5\text{V}$, $V_{GS}=-4.5\text{V}$
Drain-Source On-Resistance ¹	$R_{DS(ON)}$	N	-	-	47	m Ω	$V_{GS}=4.5\text{V}$, $I_D=5.3\text{A}$
			-	-	55		$V_{GS}=2.5\text{V}$, $I_D=5\text{A}$
		P	-	-	79		$V_{GS}=-4.5\text{V}$, $I_D=-4.2\text{A}$
			-	-	110		$V_{GS}=-2.5\text{V}$, $I_D=-3.8\text{A}$
Diode Forward Voltage	V_{SD}	N	-	0.7	V	$V_{GS}=0$, $I_S=1.1\text{A}$	
		P	-	-0.73		$V_{GS}=0$, $I_S=-1.1\text{A}$	
Forward Transconductance ¹	g_{fs}	N	-	10	-	S	$V_{DS}=10\text{V}$, $I_D=5.3\text{A}$
		P	-	10	-		$V_{DS}=-10\text{V}$, $I_D=-4.2\text{A}$
Dynamic ²							
Input Capacitance	C_{iss}	N	-	439	-	pF	N-Channel $V_{DS}=15\text{V}$, $V_{GS}=0$, $f=1\text{MHz}$ P-Channel $V_{DS}=-15\text{V}$, $V_{GS}=0$, $f=1\text{MHz}$
		P	-	683	-		
Output Capacitance	C_{oss}	N	-	78	-		
		P	-	90	-		
Reverse Transfer Capacitance	C_{rss}	N	-	68	-		
		P	-	75	-		
Total Gate Charge	Q_g	N	-	6	-	nC	
		P	-	11	-		
Gate-Source Charge	Q_{gs}	N	-	0.9	-		N-Channel $I_D=5.3\text{A}$, $V_{DS}=10\text{V}$, $V_{GS}=4.5\text{V}$
		P	-	2.8	-		
Gate-Drain Charge	Q_{gd}	N	-	2.1	-		P-Channel $I_D=-4.2\text{A}$, $V_{DS}=-10\text{V}$, $V_{GS}=-4.5\text{V}$
		P	-	2.7	-		
Turn-On Delay Time	$T_{d(on)}$	N	-	7	-	nS	
		P	-	10	-		
Rise Time	T_r	N	-	24	-		N-Channel $V_{DD}=10\text{V}$, $V_{GEN}=4.5\text{V}$ $I_D=5.3\text{A}$, $R_{GEN}=6\Omega$, $R_L=1.8\Omega$
		P	-	20	-		
Turn-Off Delay Time	$T_{d(off)}$	N	-	35	-		P-Channel $V_{DD}=-10\text{V}$, $V_{GEN}=-4.5\text{V}$ $I_D=-4.2\text{A}$, $R_{GEN}=6\Omega$, $R_L=2.3\Omega$
		P	-	49	-		
Fall Time	T_f	N	-	19	-		
		P	-	21	-		

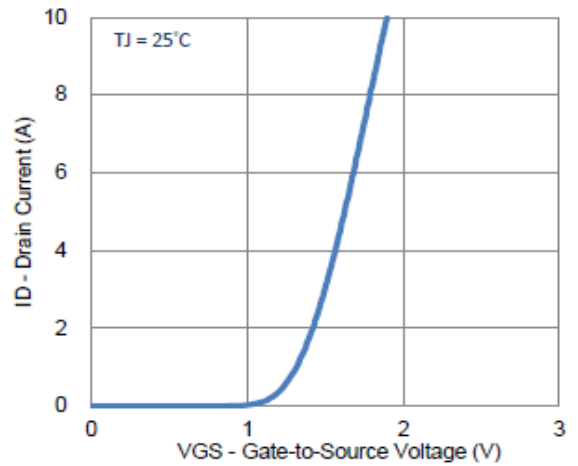
Notes:

1. Pulse test : $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
2. Guaranteed by design, not subject to production testing.

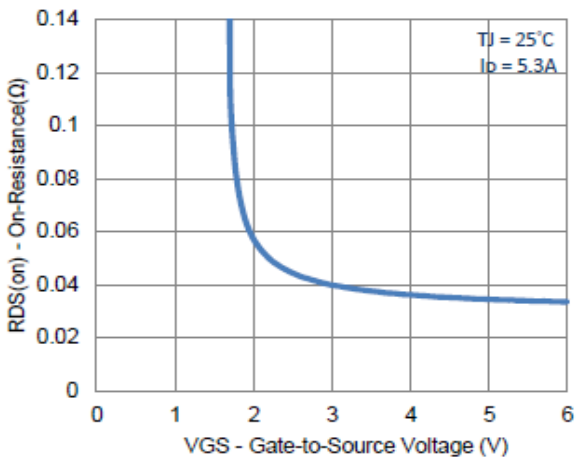
CHARACTERISTIC CURVES (N-Channel)



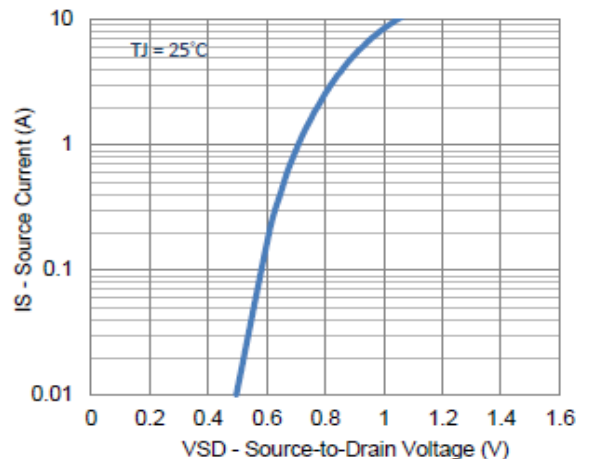
1. On-Resistance vs. Drain Current



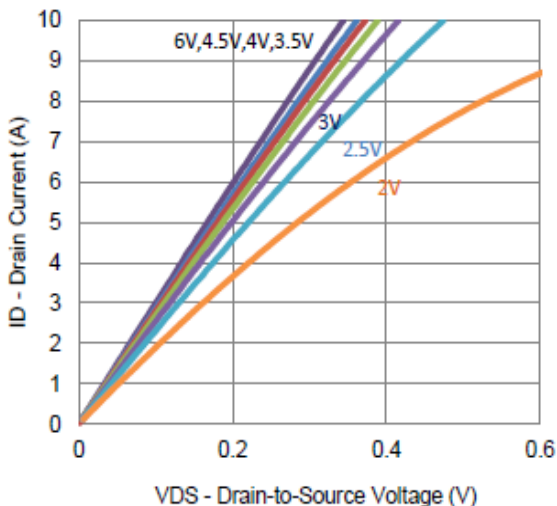
2. Transfer Characteristics



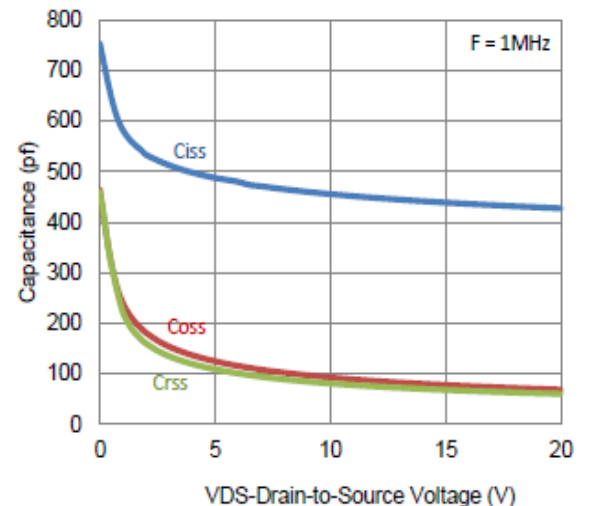
3. On-Resistance vs. Gate-to-Source Voltage



4. Drain-to-Source Forward Voltage

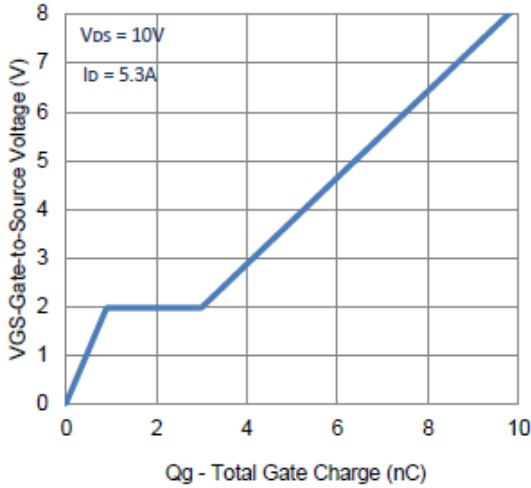


5. Output Characteristics

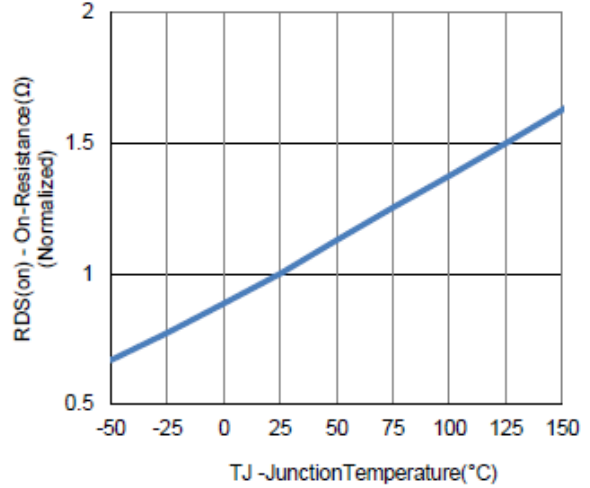


6. Capacitance

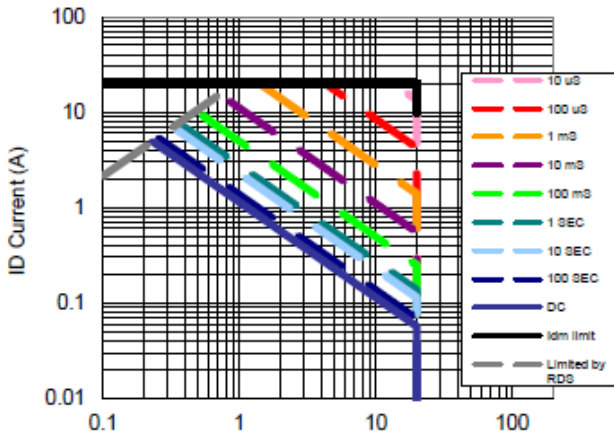
CHARACTERISTIC CURVES



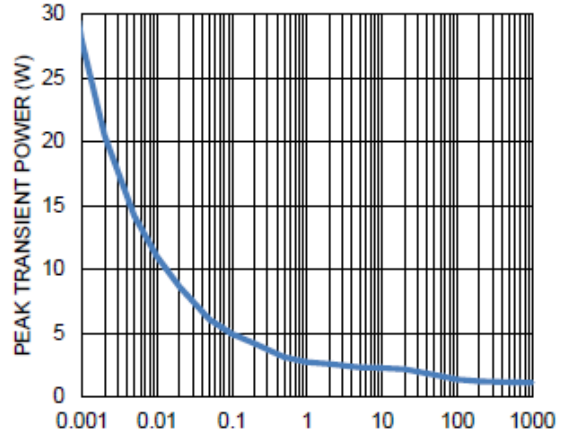
7. Gate Charge



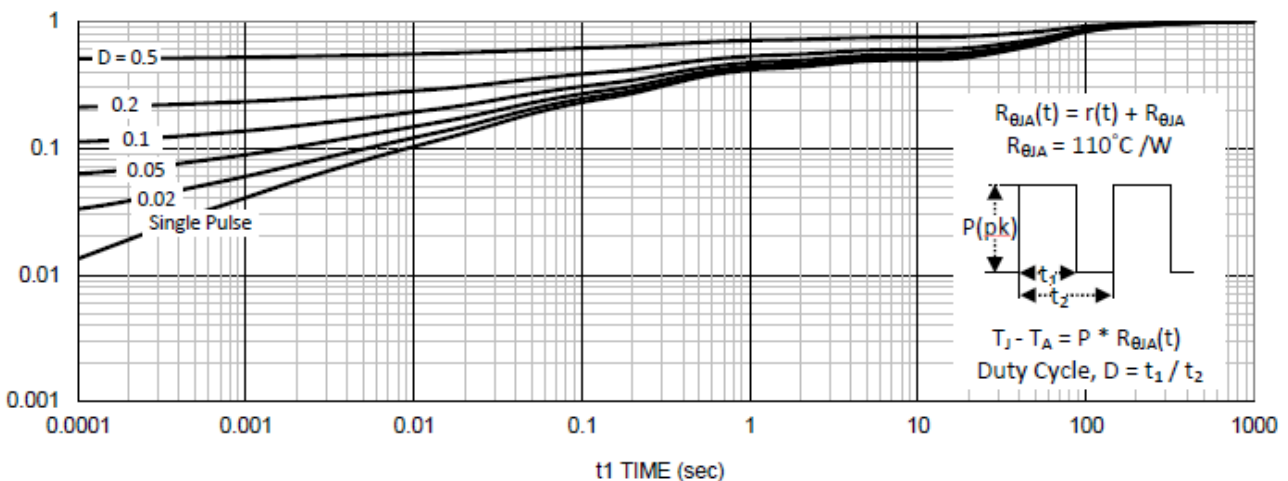
8. Normalized On-Resistance Vs Junction Temperature



9. Safe Operating Area

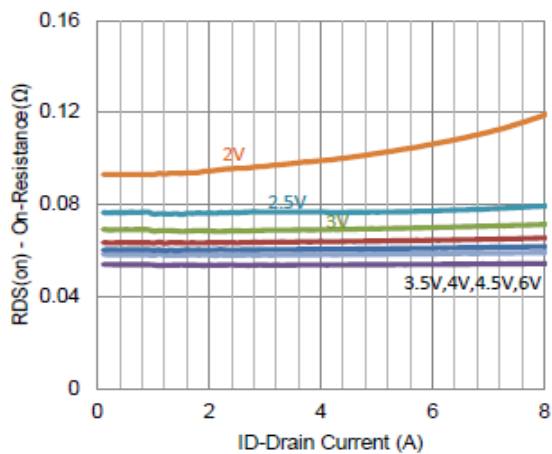


10. Single Pulse Maximum Power Dissipation

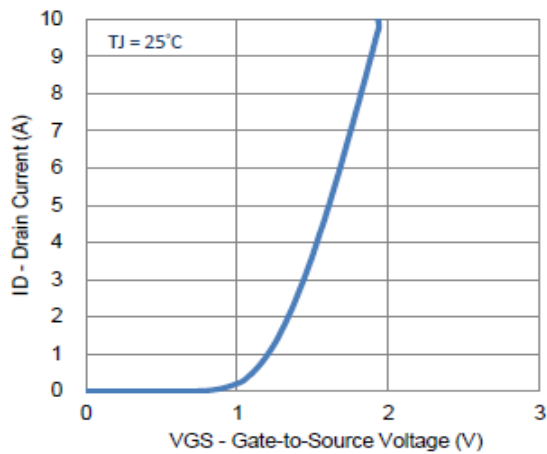


11. Normalized Thermal Transient Junction to Ambient

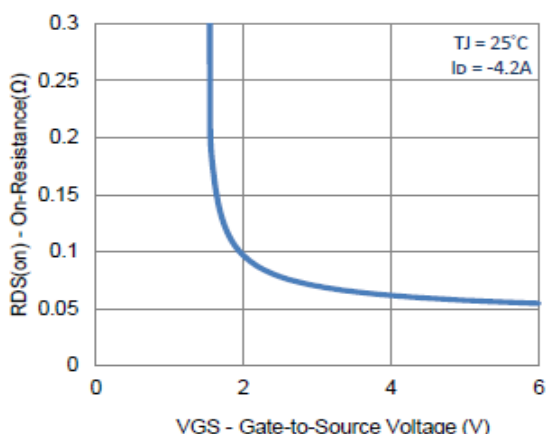
CHARACTERISTIC CURVES (P-Channel)



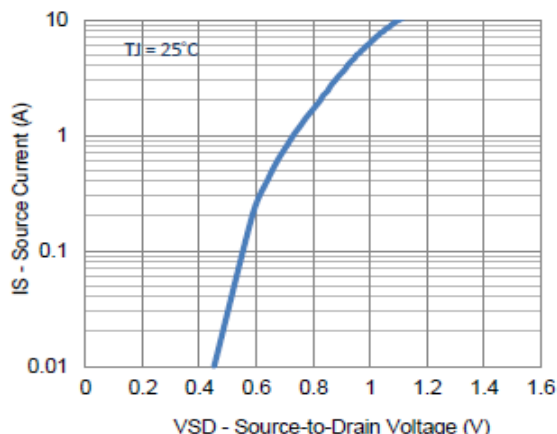
1. On-Resistance vs. Drain Current



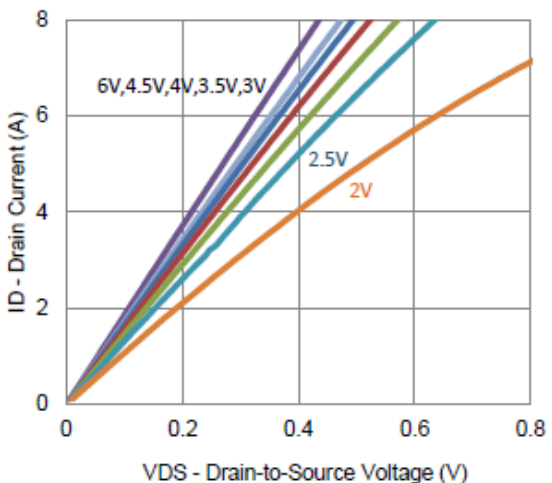
2. Transfer Characteristics



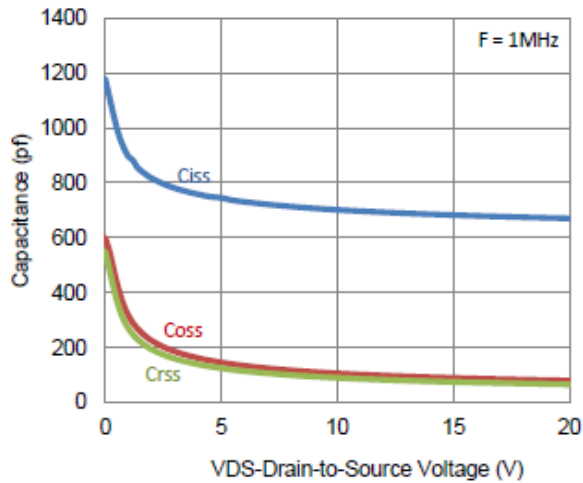
3. On-Resistance vs. Gate-to-Source Voltage



4. Drain-to-Source Forward Voltage

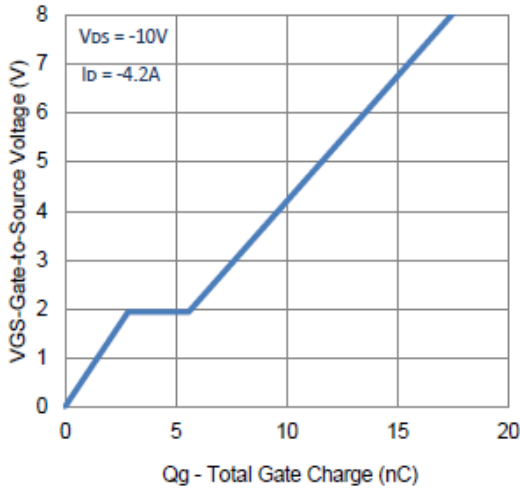


5. Output Characteristics

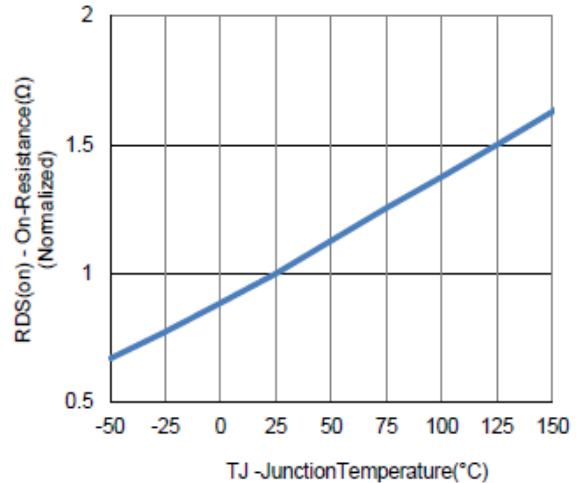


6. Capacitance

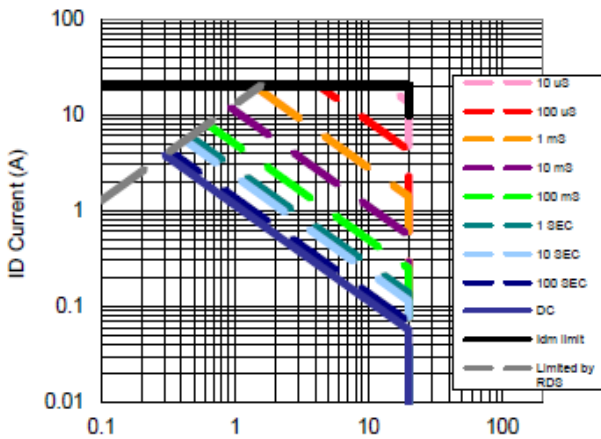
CHARACTERISTIC CURVES



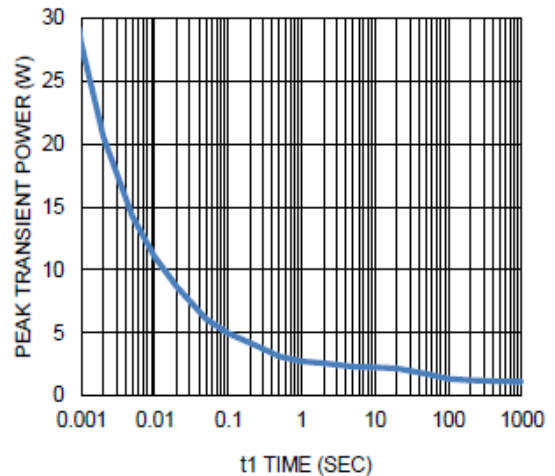
7. Gate Charge



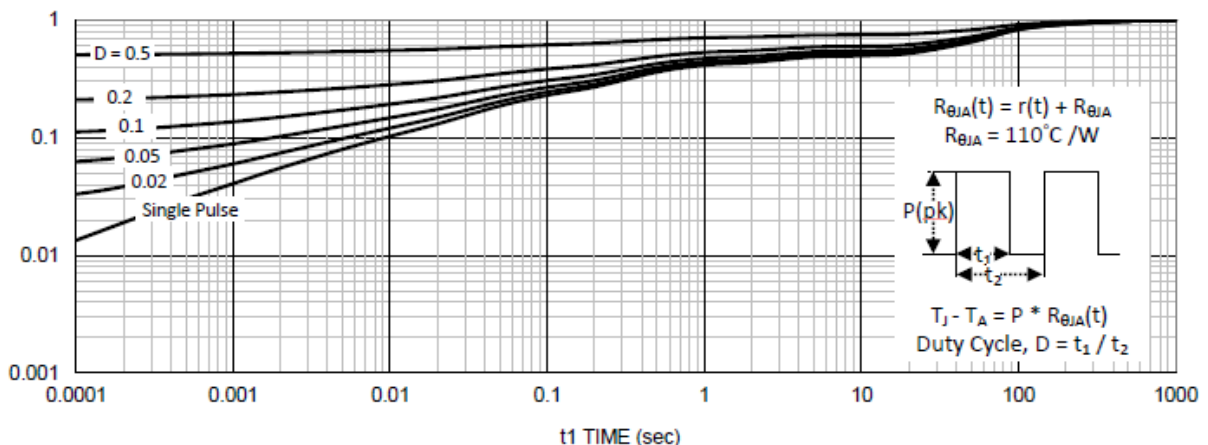
8. Normalized On-Resistance Vs Junction Temperature



9. Safe Operating Area



10. Single Pulse Maximum Power Dissipation



11. Normalized Thermal Transient Junction to Ambient