

RoHS Compliant Product
 A suffix of "-C" specifies halogen & lead-free

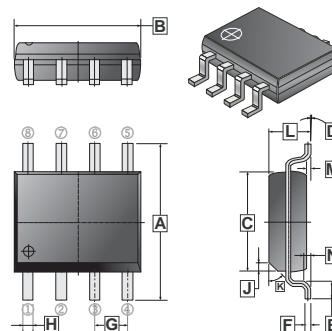
DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones

FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Low thermal impedance copper leadframe SOP-8 saves board space
- Fast switching speed
- High performance trench technology

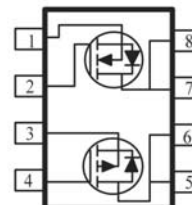
SOP-8



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.8	6.20	H	0.35	0.51
B	4.80	5.00	J	0.375 REF.	
C	3.80	4.00	K	45°	
D	0°	8°	L	1.35	1.75
E	0.50	0.93	M	0.10	0.25
F	0.19	0.25	N	0.25 REF.	
G	1.27 TYP.				

PACKAGE INFORMATION

Package	MPQ	LeaderSize
SOP-8	2.5K	13' inch



MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	N-CH	P-CH	Unit
Drain-Source Voltage	V_{DS}	40	-40	V
Gate-Source Voltage	V_{GS}	20	-20	V
Continuous Drain Current ¹	$I_D @ T_A = 25^\circ\text{C}$	6.5	-7.6	A
	$I_D @ T_A = 70^\circ\text{C}$	5.5	-6.3	A
Pulsed Drain Current ²	I_{DM}	± 50	± 50	A
Continuous Source Current (Diode Conduction) ¹	I_S	2.3	-2.1	A
Total Power Dissipation ¹	$P_D @ T_A = 25^\circ\text{C}$	2.1	2.1	W
	$P_D @ T_A = 70^\circ\text{C}$	1.3	1.3	W
Operating Junction & Storage Temperature Range	T_J, T_{STG}	-55 ~ 150		$^\circ\text{C}$
Thermal Resistance Ratings				
Maximum Junction-to-Ambient ¹	$t \leq 10$ sec	$R_{\theta JA}$	62.5	$^\circ\text{C} / \text{W}$
	Steady State		110	$^\circ\text{C} / \text{W}$

Notes

1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

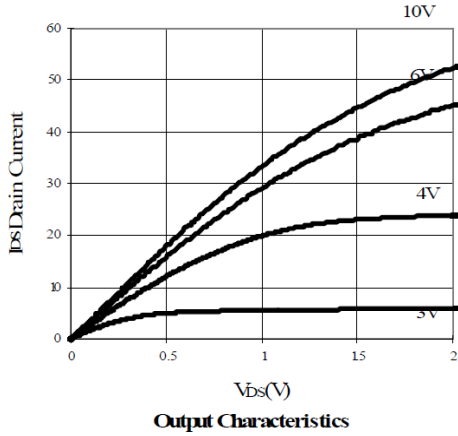
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Ch	Min.	Typ.	Max.	Unit	Test Conditions
Static							
Gate Threshold Voltage	V _{GS(th)}	N	1	-	-	V	V _{DS} = V _{GS} , I _D = 250μA
		P	-1	-	-		V _{DS} = V _{GS} , I _D = -250μA
Gate-Body Leakage Current	I _{GSS}	N	-	-	±100	nA	V _{DS} = 0V, V _{GS} = 20V
		P	-	-	±100		V _{DS} = 0V, V _{GS} = -20V
Zero Gate Voltage Drain Current	I _{DSS}	N	-	-	1	μA	V _{DS} = 32V, V _{GS} = 0V
		P	-	-	-1		V _{DS} = -32V, V _{GS} = 0V
On-State Drain Current ¹	I _{D(on)}	N	25	-	-	A	V _{DS} = 5V, V _{GS} = 10V
		P	-50	-	-		V _{DS} = -5V, V _{GS} = -10V
Drain-Source On-Resistance ¹	R _{DS(ON)}	N	-	-	32	mΩ	V _{GS} = 10V, I _D = 6.5A
			-	-	42		V _{GS} = 4.5V, I _D = 5.7A
		P	-	-	30		V _{GS} = -10V, I _D = -7.6A
			-	-	40		V _{GS} = -4.5V, I _D = -6.2A
Forward Transconductance ¹	g _{fs}	N	-	40	-	S	V _{DS} = 15V, I _D = 6.5A
		P	-	31	-		V _{DS} = -15V, I _D = -7.6A
Dynamic ²							
Total Gate Charge	Q _g	N	-	13	-	nC	N-Channel I _D = 6.5A, V _{DS} = 15V, V _{GS} = 4.5V P-Channel I _D = -7.6A, V _{DS} = -15V, V _{GS} = -4.5V
		P	-	14	-		
Gate-Source Charge	Q _{gs}	N	-	3.3	-	nC	N-Channel I _D = 6.5A, V _{DS} = 15V, V _{GS} = 4.5V P-Channel I _D = -7.6A, V _{DS} = -15V, V _{GS} = -4.5V
		P	-	5.8	-		
Gate-Drain Charge	Q _{gd}	N	-	4.5	-	nC	N-Channel I _D = 6.5A, V _{DS} = 15V, V _{GS} = 4.5V P-Channel I _D = -7.6A, V _{DS} = -15V, V _{GS} = -4.5V
		P	-	12	-		
Input Capacitance	C _{ISS}	N	-	440	-	pF	N-Channel V _{DS} = 15V, V _{GS} = 0V, f = 1MHz P-Channel V _{DS} = -15V, V _{GS} = 0V, f = 1MHz
		P	-	1800	-		
Output Capacitance	C _{OSS}	N	-	80	-	pF	N-Channel V _{DS} = 15V, V _{GS} = 0V, f = 1MHz P-Channel V _{DS} = -15V, V _{GS} = 0V, f = 1MHz
		P	-	280	-		
Reverse Transfer Capacitance	C _{RSS}	N	-	130	-	pF	N-Channel V _{DS} = 15V, V _{GS} = 0V, f = 1MHz P-Channel V _{DS} = -15V, V _{GS} = 0V, f = 1MHz
		P	-	150	-		
Turn-On Delay Time	T _{d(on)}	N	-	20	-	nS	N-Channel V _{DD} = 15V, V _{GS} = 10V I _D = 1A, R _{GEN} = 25Ω P-Channel V _{DD} = -15V, V _{GS} = -10V I _D = -1A, R _{GEN} = 15Ω
		P	-	15	-		
Rise Time	T _r	N	-	9	-	nS	N-Channel V _{DD} = 15V, V _{GS} = 10V I _D = 1A, R _{GEN} = 25Ω P-Channel V _{DD} = -15V, V _{GS} = -10V I _D = -1A, R _{GEN} = 15Ω
		P	-	16	-		
Turn-Off Delay Time	T _{d(off)}	N	-	70	-	nS	N-Channel V _{DD} = 15V, V _{GS} = 10V I _D = 1A, R _{GEN} = 25Ω P-Channel V _{DD} = -15V, V _{GS} = -10V I _D = -1A, R _{GEN} = 15Ω
		P	-	62	-		
Fall Time	T _f	N	-	20	-	nS	N-Channel V _{DD} = 15V, V _{GS} = 10V I _D = 1A, R _{GEN} = 25Ω P-Channel V _{DD} = -15V, V _{GS} = -10V I _D = -1A, R _{GEN} = 15Ω
		P	-	46	-		

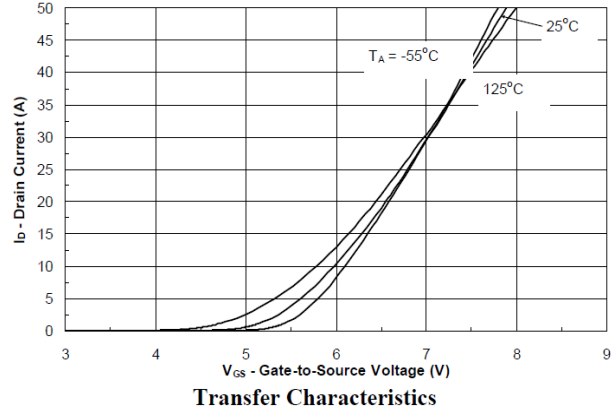
Notes

- Pulse test : PW ≤ 300μs duty cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.

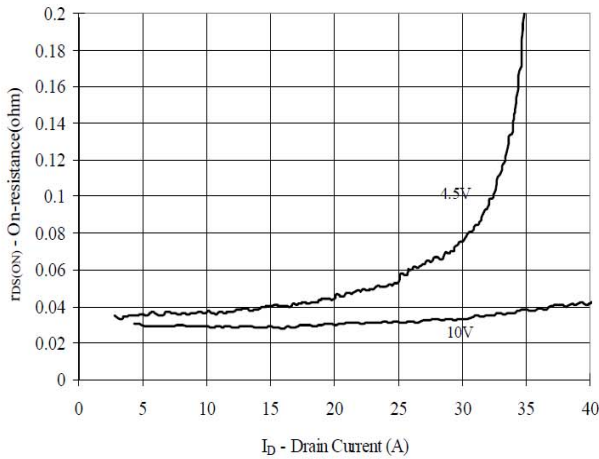
CHARACTERISTIC CURVES (N-Channel)



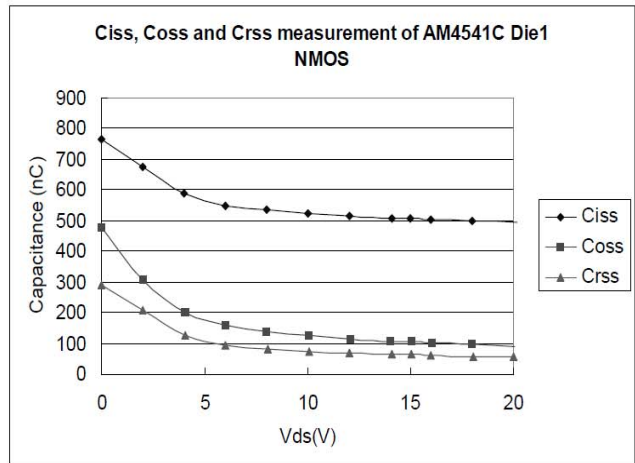
Output Characteristics



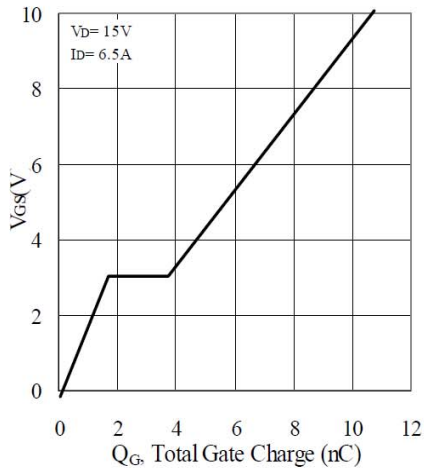
Transfer Characteristics



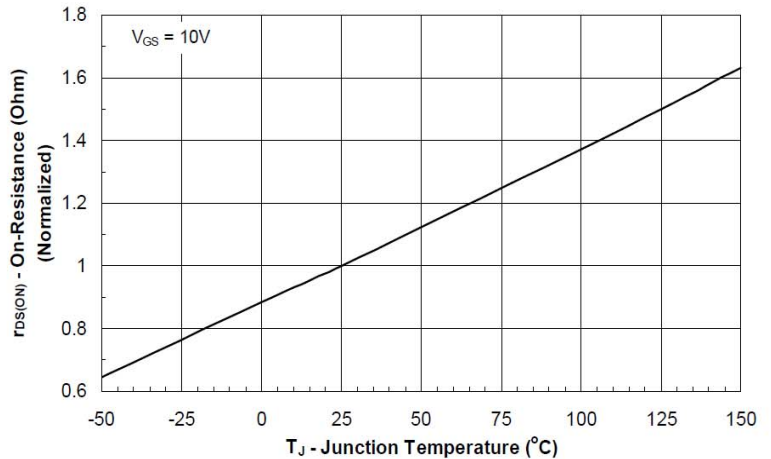
On Resistance vs. Drain Current



Capacitance

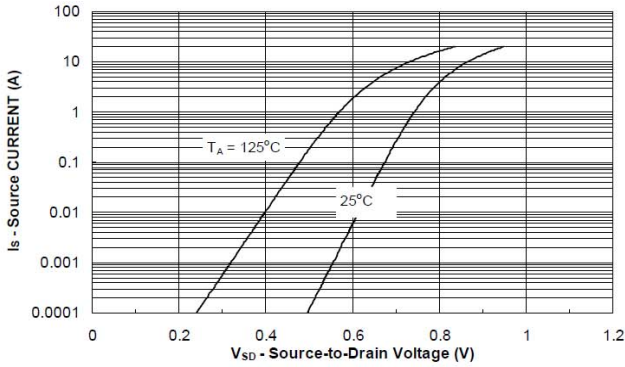


Gate Charge

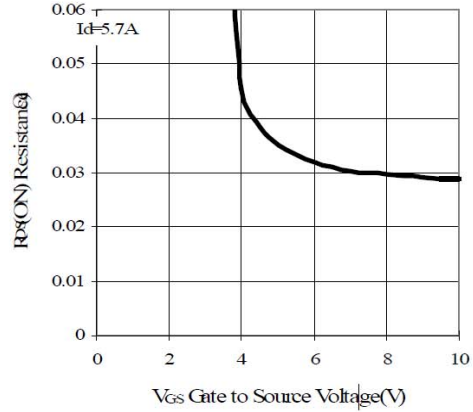


On-Resistance vs. Junction Temperature

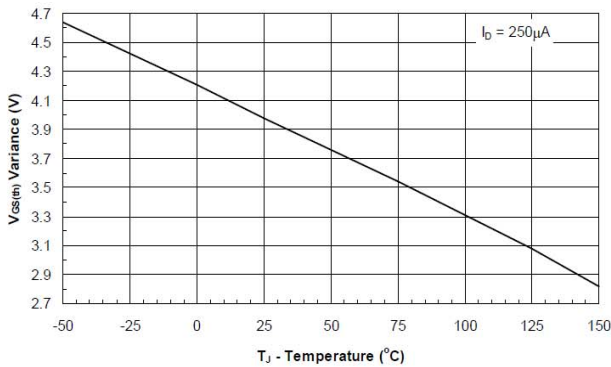
CHARACTERISTIC CURVES



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

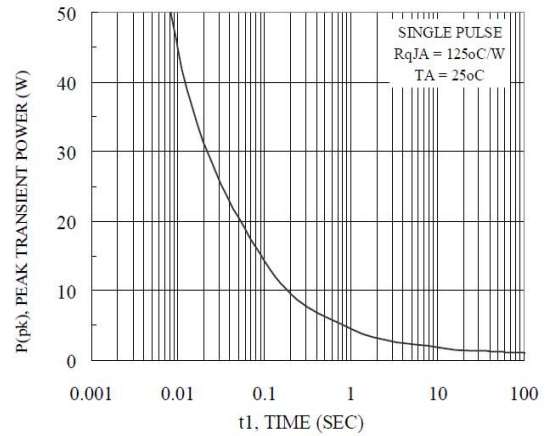


Figure 10. Single Pulse Maximum Power Dissipation

Normalized Thermal Transient Junction to Ambient

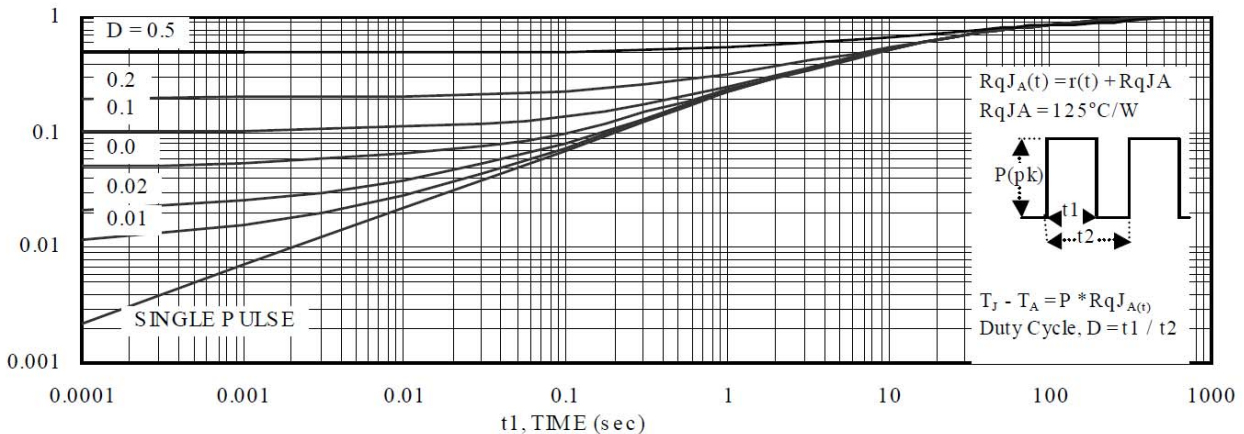
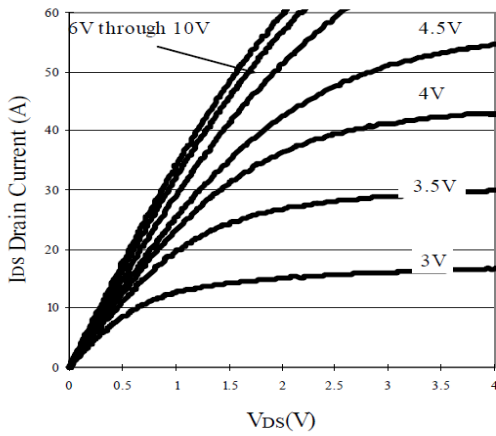
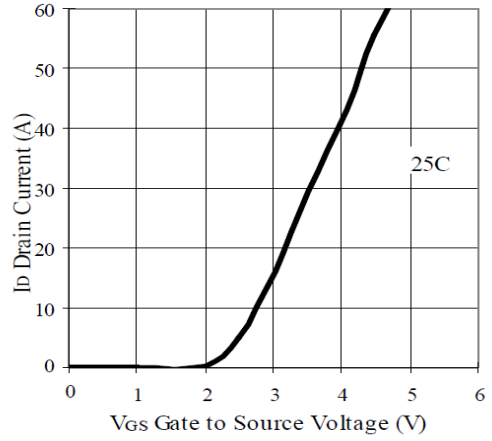


Figure 11. Transient Thermal Response Curve

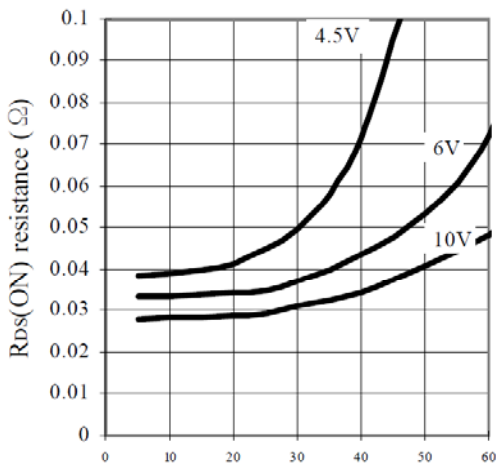
CHARACTERISTIC CURVES (P-Channel)



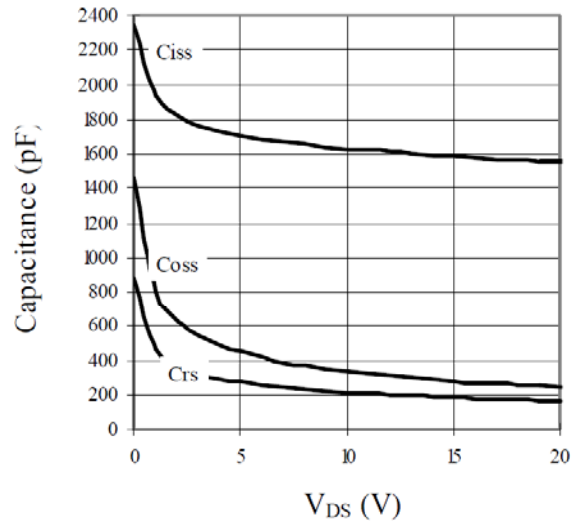
Output Characteristics



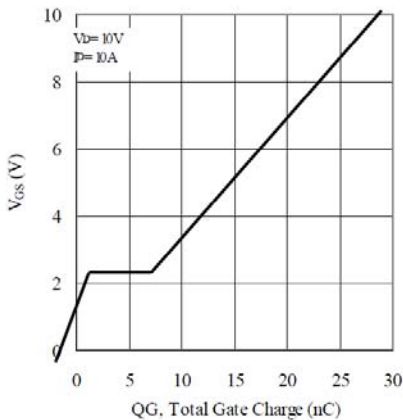
Transfer Characteristics



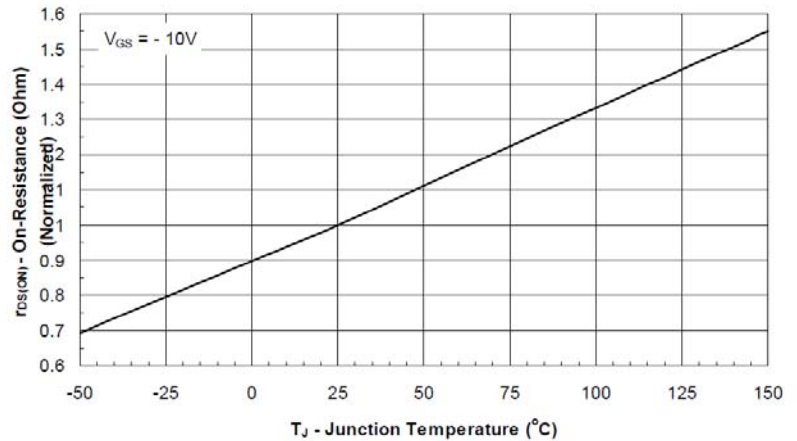
On Resistance Vs Vgs Voltage



Capacitance

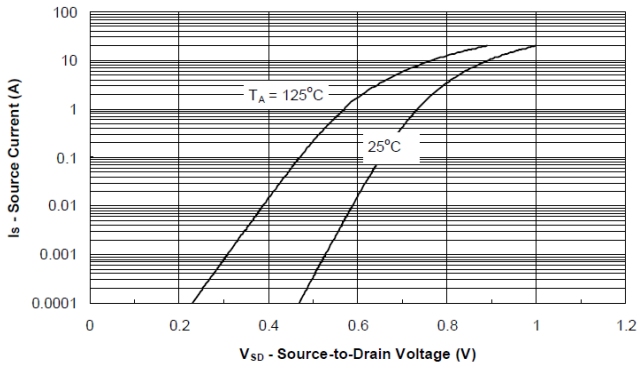


Gate Charge

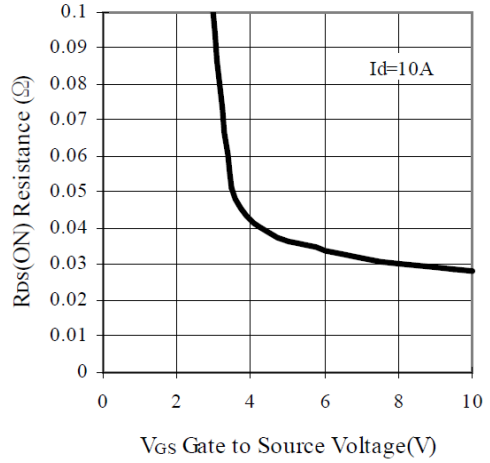


On-Resistance vs. Junction Temperature

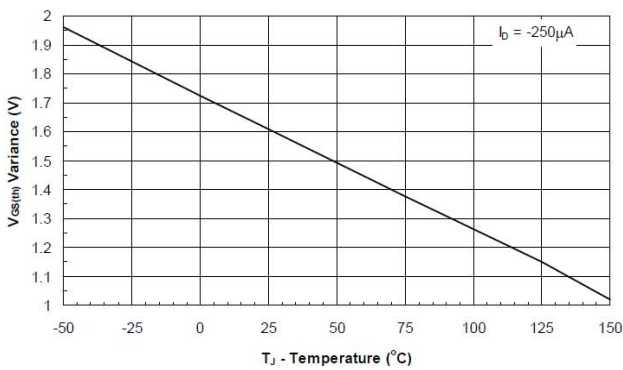
CHARACTERISTIC CURVES



Source-Drain Diode Forward Voltage



On-Resistance with Gate to Source Voltage



Threshold Voltage

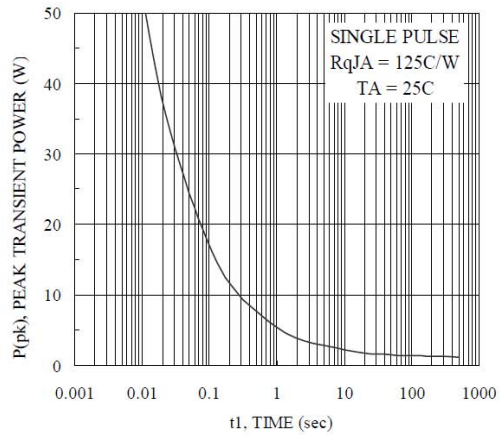


Figure 10. Single Pulse Maximum Power Dissipation

Normalized Thermal Transient Junction to Ambient

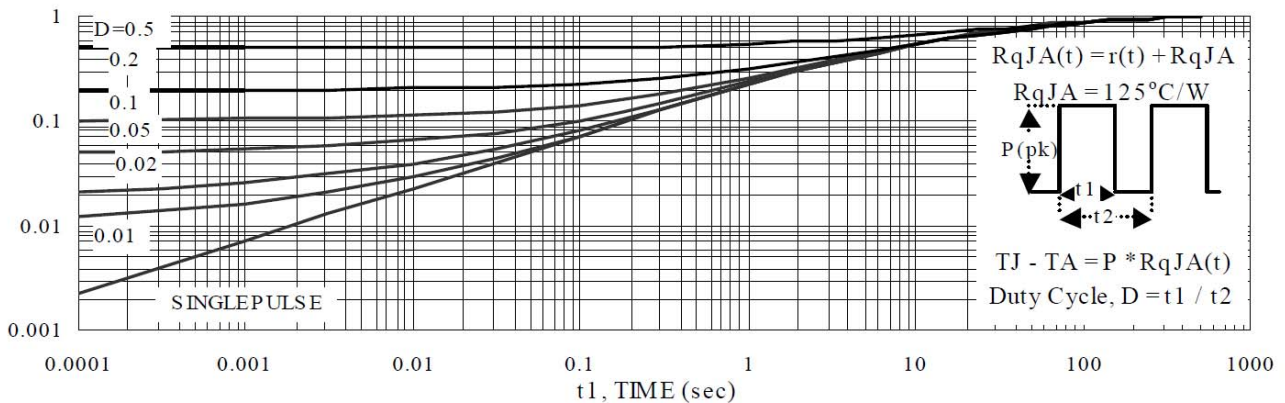


Figure 11. Transient Thermal Response Curve