Elektronische Bauelemente

SSG6560-C

N-Ch: 4.5A, 60V, $R_{DS(ON)}$ 45 mΩ
P-Ch: -3.5A, -60V, $R_{DS(ON)}$ 80 mΩ
N & P-Ch Enhancement Mode Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

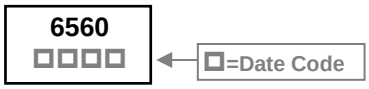
The SSG6560-C is the highest performance trench N-Ch and P-Ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The SSG6560-C meet the RoHS and Green Product requirement with full function reliability approved.

FEATURES

- Advanced High Cell Density Trench Technology
- Super Low Gate Charge
- Green Device Available

MARKING



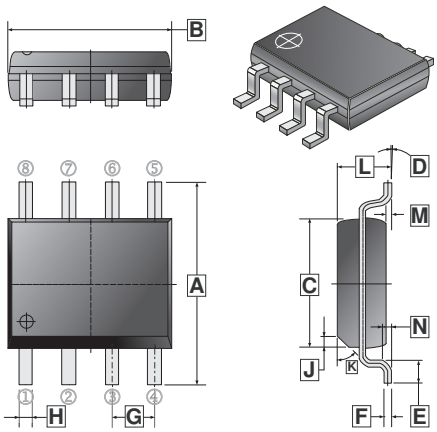
PACKAGE INFORMATION

Package	MPQ	Leader Size
SOP-8	2.5K	13 inch

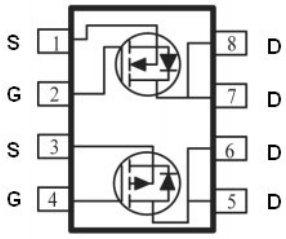
ORDER INFORMATION

Part Number	Type
SSG6560-C	Lead (Pb)-free and Halogen-free

SOP-8



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.79	6.20	H	0.33	0.51
B	4.70	5.11	J	0.375 REF.	
C	3.80	4.00	K	45°REF.	
D	0°	8°	L	1.3	1.752
E	0.40	1.27	M	0	0.25
F	0.10	0.25	N	0.25 REF.	
G	1.27 TYP.				



ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Ratings		Unit
			N-Ch	P-Ch	
Drain-Source Voltage		V_{DS}	60	-60	V
Gate-Source Voltage		V_{GS}	±20		V
Continuous Drain Current, @V_{GS}=10V [1]	T_A=25℃	I_D	4.5	-3.5	A
	T_A=70℃		3.6	-2.8	
Pulsed Drain Current [3]		I_{DM}	20	-20	A
Total Power Dissipation	T_A=25℃	P_D	1.5		W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150		℃
Thermal Data					
Thermal Resistance Junction-Ambient [1]		$R_{\theta JA}$	t≦10sec, 83		℃/W
			Steady State, 125		
Thermal Resistance Junction-Ambient [2]			135		
Thermal Resistance Junction-Case [1]		$R_{\theta JC}$	40		

N-CHANNEL ELECTRICAL CHARACTERISTICS (T_J=25℃ unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		BV_{DSS}	60	-	-	V	V_{GS}=0, I_D=250μA
Gate Threshold Voltage		$V_{GS(th)}$	1	-	2.5	V	V_{DS}=V_{GS}, I_D=250μA
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current	T_J=25℃	I_{DSS}	-	-	1	μA	V_{DS}=48V, V_{GS}=0
	T_J=55℃		-	-	5		
Forward Transfer Conductance		g_{fs}	-	25.3	-	S	V_{DS}=5V, I_D=4A
Static Drain-Source On-Resistance [2]		$R_{DS(ON)}$	-	-	45	mΩ	V_{GS}=10V, I_D=4.5A
			-	-	55		V_{GS}=4.5V, I_D=4A
Total Gate Charge [2]		Q_g	-	19	-	nC	I_D=4.5A V_{DS}=48V V_{GS}=10V
Gate-Source Charge		Q_{gs}	-	2.5	-		
Gate-Drain ("Miller") Change		Q_{gd}	-	5	-		
Turn-on Delay Time [2]		$T_{d(on)}$	-	2.8	-	nS	V_{DS}=30V I_D=4.5A V_{GS}=10V R_G=3.3Ω
Rise Time		T_r	-	16.6	-		
Turn-off Delay Time		$T_{d(off)}$	-	21.2	-		
Fall Time		T_f	-	5.6	-		
Input Capacitance		C_{iss}	-	1027	-	pF	V_{GS}=0 V_{DS}=15V f=1MHz
Output Capacitance		C_{oss}	-	65	-		
Reverse Transfer Capacitance		C_{rss}	-	46	-		
Source-Drain Diode							
Forward on Voltage [4]		V_{SD}	-	-	1.2	V	I_S=1A, V_{GS}=0, T_J=25℃
Continuous Source Current [1]		I_S	-	-	4.5	A	
Pulsed Source Current [3]		I_{SM}	-	-	20		

Notes:
1. Surface Mounted on 1" x 1" FR4 Board with 2OZ copper.
2. When mounted on Min. copper pad.
3. Pulse width limited by maximum junction temperature, Pulse Width ≤300μs, Duty Cycle≤2%.
4. Pulse Test: Pulse Width ≤300μs, Duty Cycle≤2%.

P-CHANNEL ELECTRICAL CHARACTERISTICS (T_J=25℃ unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		BV_{DSS}	-60	-	-	V	V_{GS}=0, I_D= -250μA
Gate Threshold Voltage		$V_{GS(th)}$	-1	-	-2.5	V	V_{DS}=V_{GS}, I_D= -250μA
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current	T_J=25℃	I_{DSS}	-	-	-1	μA	V_{DS}= -48V, V_{GS}=0
	T_J=55℃		-	-	-5		
Forward Transfer Conductance		g_{fs}	-	8.7	-	S	V_{DS}= -5V, I_D= -3.5A
Static Drain-Source On-Resistance [2]		$R_{DS(ON)}$	-	-	80	mΩ	V_{GS}= -10V, I_D= -3.5A
			-	-	105		V_{GS}= -4.5V, I_D= -3A
Total Gate Charge [2]		Q_g	-	11.8	-	nC	I_D= -3.5A V_{DS}= -48V V_{GS}= -4.5V
Gate-Source Charge		Q_{gs}	-	1.9	-		
Gate-Drain (“Miller”) Change		Q_{gd}	-	6.5	-		
Turn-on Delay Time		$T_{d(on)}$	-	8.8	-	nS	V_{DS}= -30V I_D= -3.5A V_{GS}= -10V R_G=3.3Ω
Rise Time		T_r	-	19.6	-		
Turn-off Delay Time		$T_{d(off)}$	-	47.2	-		
Fall Time		T_f	-	9.6	-		
Input Capacitance		C_{iss}	-	1080	-	pF	V_{GS}=0 V_{DS}= -15V f=1MHz
Output Capacitance		C_{oss}	-	97	-		
Reverse Transfer Capacitance		C_{rss}	-	50	-		
Source-Drain Diode							
Forward on Voltage [4]		V_{SD}	-	-	-1.2	V	V_{GS}=0, I_S= -1A, T_J=25℃
Continuous Source Current [1]		I_S	-	-	-3.5	A	
Pulsed Source Current [3]		I_{SM}	-	-	-20		

Notes:
1. Surface Mounted on 1” x 1” FR4 Board with 2OZ copper.
2. When mounted on Min. copper pad.
3. Pulse width limited by maximum junction temperature, Pulse Width ≤300μs, Duty Cycle≤2%.
4. Pulse Test: Pulse Width ≤300μs, Duty Cycle≤2%.

N-CHANNEL CHARACTERISTIC CURVE

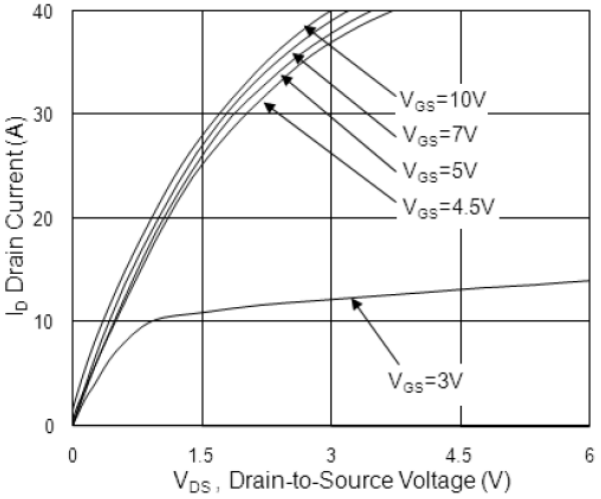


Fig.1 Typical Output Characteristics

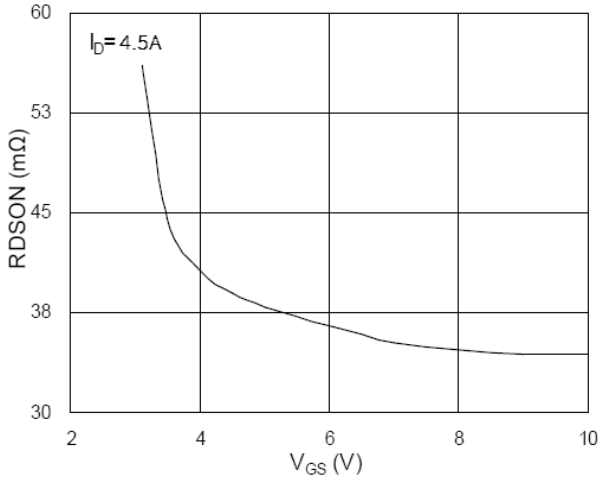


Fig.2 On-Resistance vs. Gate-Source

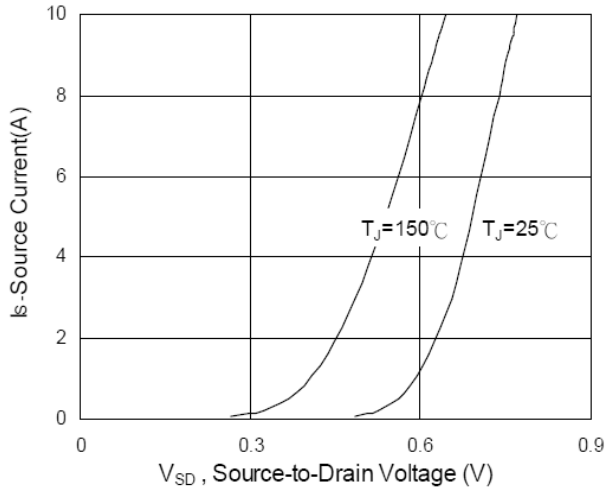


Fig.3 Forward Characteristics Of Reverse

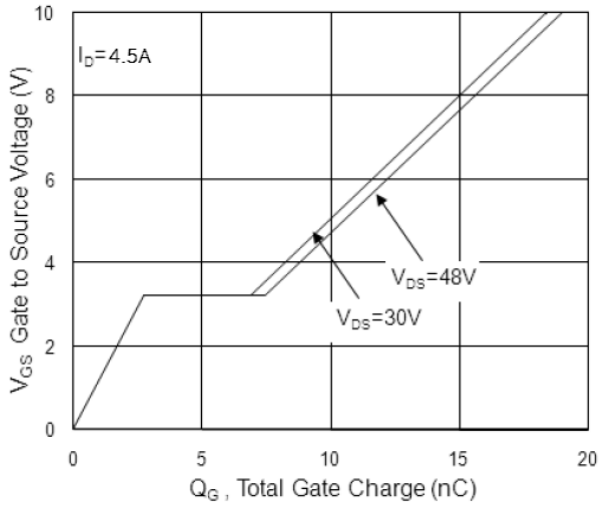


Fig.4 Gate-Charge Characteristics

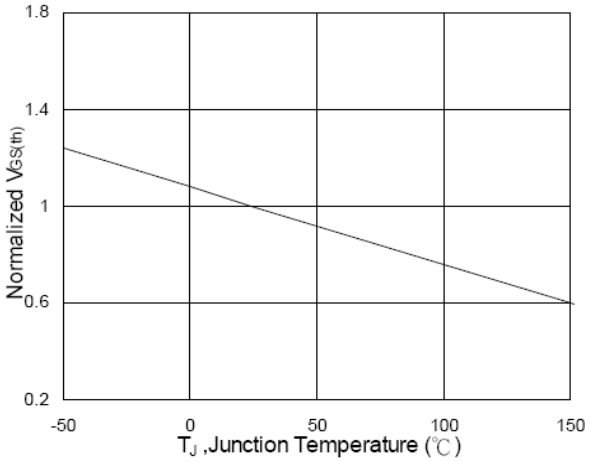


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

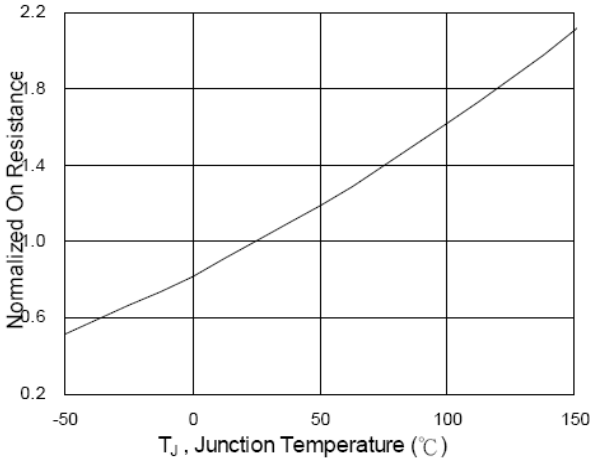


Fig.6 Normalized R_{DSON} vs. T_J

N-CHANNEL CHARACTERISTIC CURVE

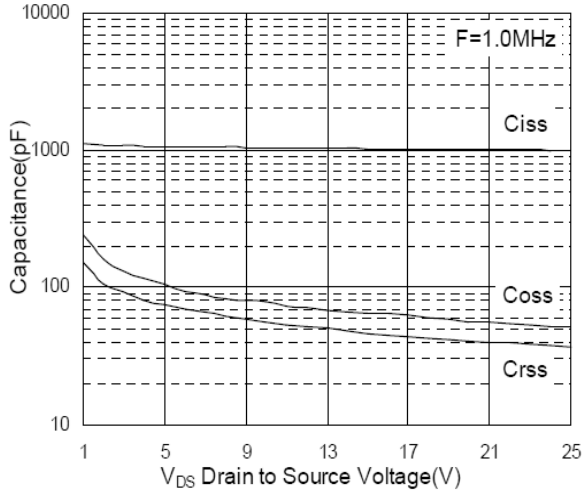


Fig.7 Capacitance

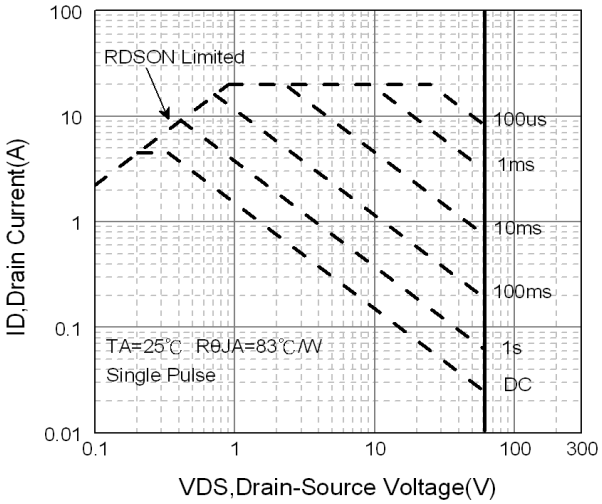


Fig.8 Safe Operating Area

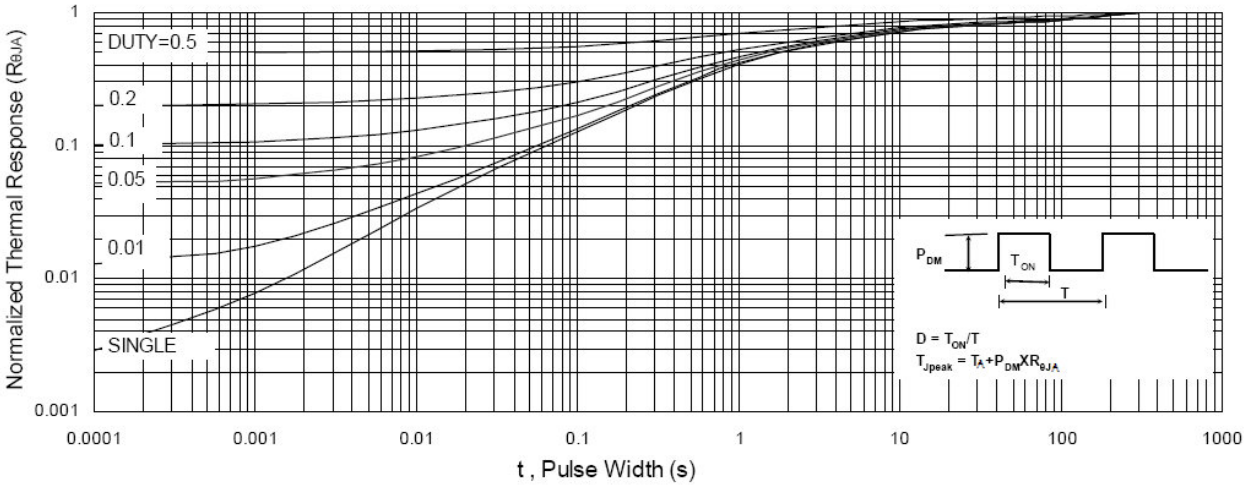


Fig.9 Normalized Maximum Transient Thermal Impedance

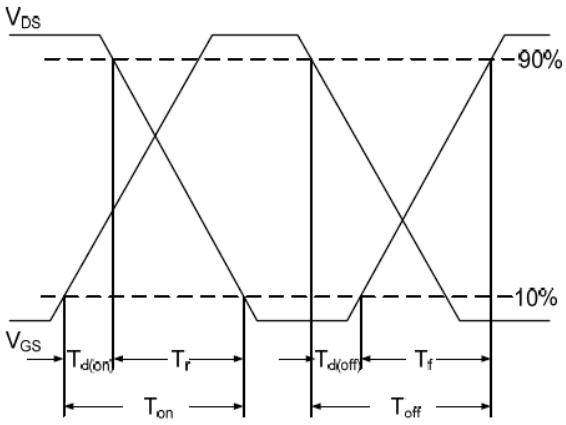


Fig.10 Switching Time Waveform

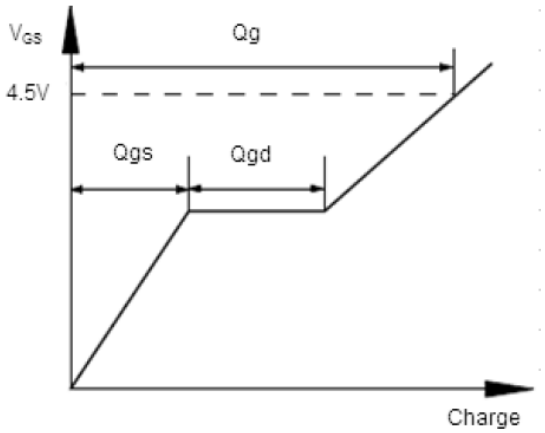


Fig.11 Gate Charge Waveform

P-CHANNEL CHARACTERISTIC CURVE

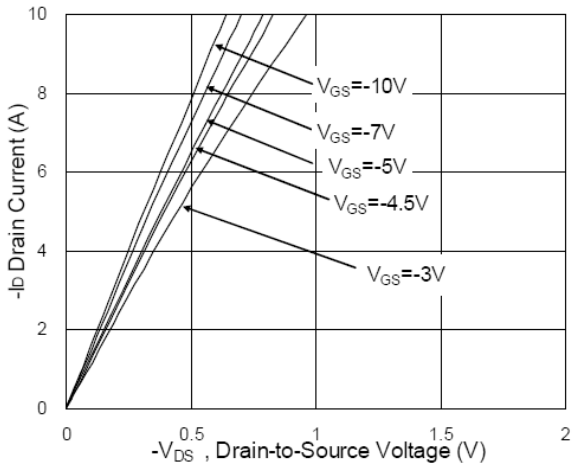


Fig.1 Typical Output Characteristics

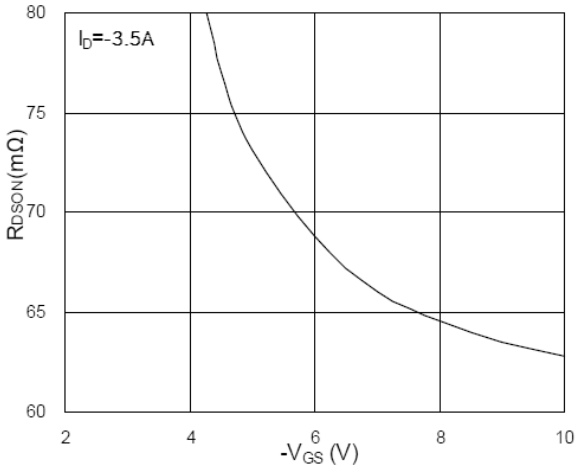


Fig.2 On-Resistance v.s Gate-Source

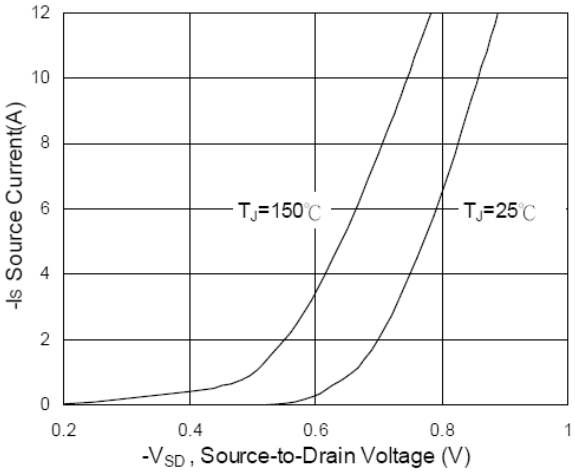


Fig.3 Forward Characteristics of Reverse

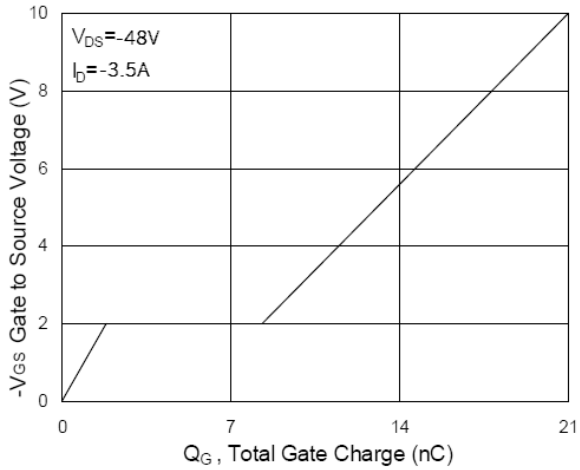


Fig.4 Gate-Charge Characteristics

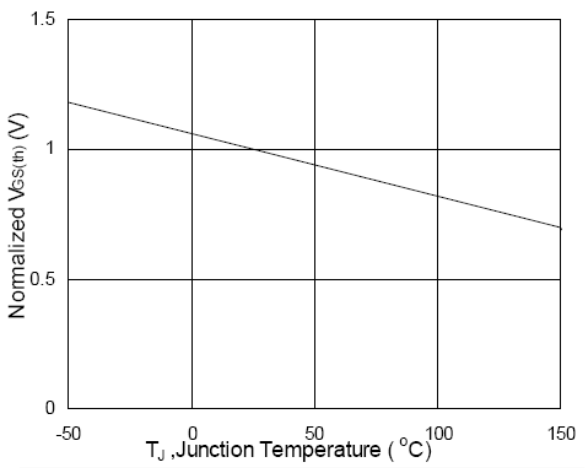


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

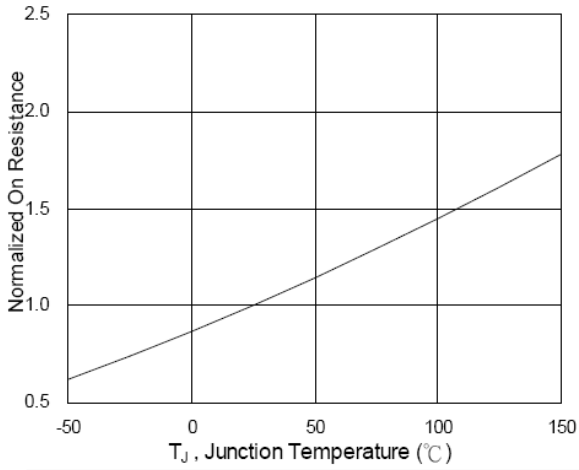


Fig.6 Normalized R_{DSON} v.s T_J

P-CHANNEL CHARACTERISTIC CURVE

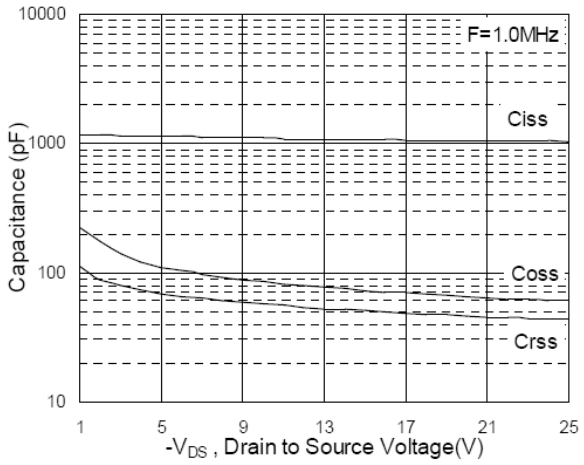


Fig.7 Capacitance

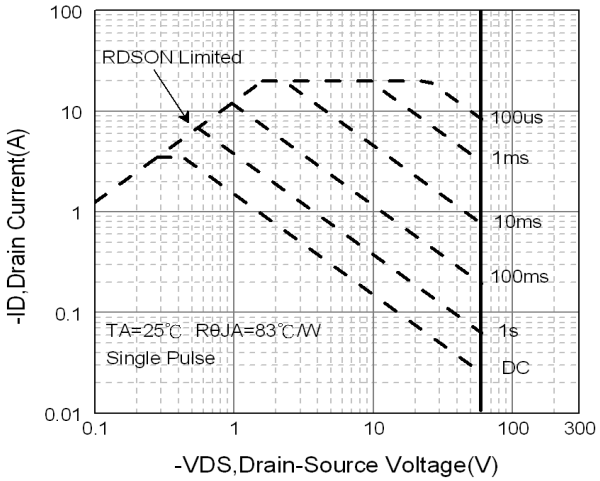


Fig.8 Safe Operating Area

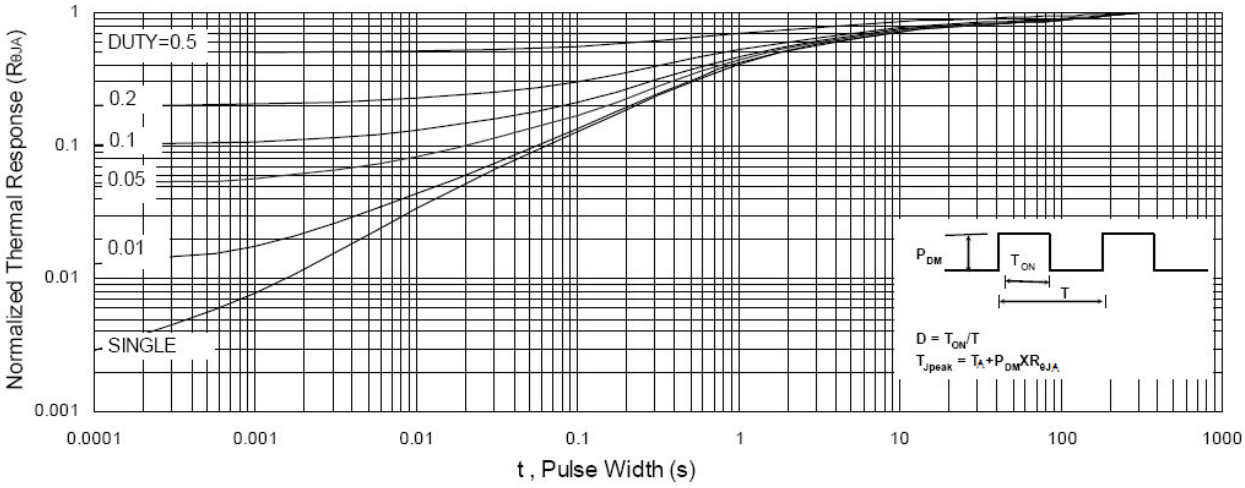


Fig.9 Normalized Maximum Transient Thermal Impedance

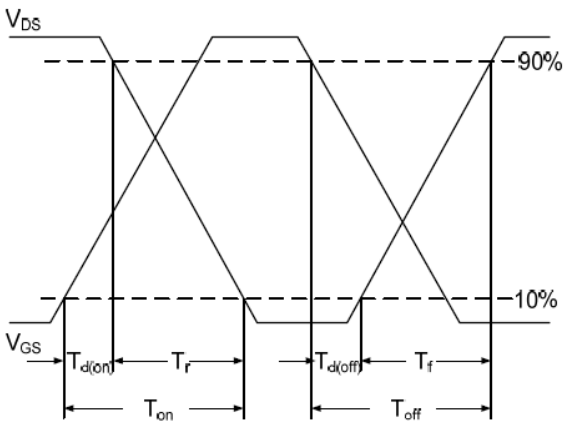


Fig.10 Switching Time Waveform

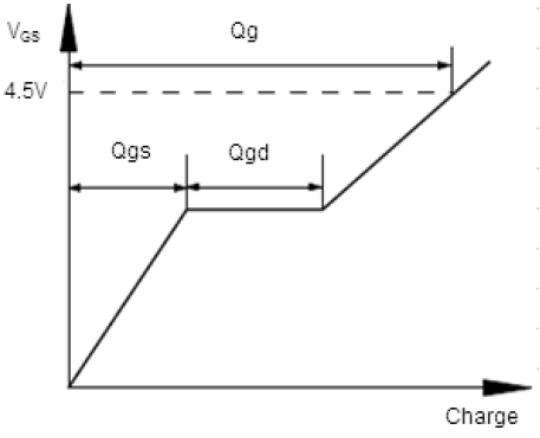


Fig.11 Gate Charge Waveform