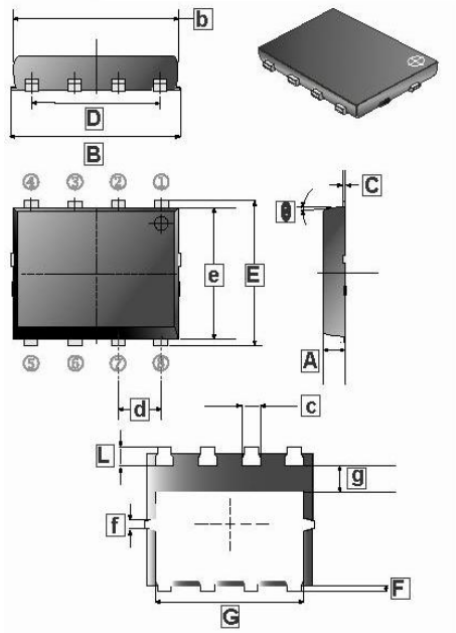
Elektronische Bauelemente

SSP7480N

12 A, 80 V, $R_{DS(ON)}$ 26 mΩ
N-Channel Enhancement MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

SOP-8PP



DESCRIPTION

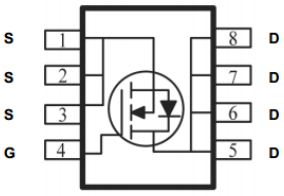
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Low thermal impedance copper leadframe SOP-8PP saves board space.
- Fast switching speed.
- High performance trench technology.

PACKAGE INFORMATION

Package	MPQ	Leader Size
SOP-8PP	3K	13 inch



REF.	Millimeter Min.	Millimeter Max.	REF.	Millimeter Min.	Millimeter Max.
A	0.85	1.00	θ	0°	10°
B	5.3 BSC.		b	5.2 BCS	
C	0.15	0.25	c	0.30	0.50
D	3.8 BCS.		d	1.27BSC	
E	6.05 BCS.		e	5.55 BCS.	
F	0.03	0.30	f	0.10	0.40
G	4.35 BCS.		g	1.2 BCS.	
L	0.40	0.70			

ABSOLUTE MAXIMUM RATINGS AND THERMAL DATA(T_A = 25°C unless otherwise specified)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	80	V
Gate-Source Voltage		V_{GS}	20	V
Continuous Drain Current [1]	T_A=25°C	I_D	12	A
	T_A=70°C		9	
Pulsed Drain Current [2]		I_{DM}	50	A
Continuous Source Current (Diode Conduction) [1]		I_S	2.3	A
Power Dissipation [1]	T_A=25°C	P_D	5.0	W
	T_A=70°C		3.2	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 ~ 150	°C
Thermal Resistance Data				
Maximum Junction to Ambient [1]	t≦10 sec	$R_{\theta JA}$	25	°C / W
	Steady-State		65	

Notes
1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	1	-	-	V	V_{DS} = V_{GS}, I_D = 250μA
Gate-Body Leakage	I_{GSS}	-	-	100	nA	V_{DS} = 0V, V_{GS}= 12V
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1	μA	V_{DS} = 64V, V_{GS}= 0V
		-	-	5		V_{DS} = 64V, V_{GS}= 0V, T_J=55°C
On-State Drain Current [1]	$I_{D(ON)}$	40	-	-	A	V_{DS} = 5V, V_{GS}= 10V
Drain-Source On-Resistance [1]	$R_{DS(ON)}$	-	-	26	mΩ	V_{GS}= 10V, I_D = 6A
		-	-	36		V_{GS}= 4.5V, I_D = 5A
Forward Transconductance [1]	g_{FS}	-	40	-	S	V_{DS}= 15V,,I_D = 6A
Diode Forward Voltage	V_{SD}	-	0.7	-	V	I_S= 2.3A, V_{GS}= 0V
Dynamic [2]						
Total Gate Charge	Q_g	-	15	-	nC	I_D= 6A V_{DS}= 15V V_{GS}= 4.5V
Gate-Source Charge	Q_{gs}	-	3	-		
Gate-Drain Charge	Q_{gd}	-	5	-		
Turn-On Delay Time	$Td_{(ON)}$	-	15	-	nS	I_D= 1A, V_{DD}= 15V V_{GEN}= 10V R_L= 6Ω
Rise Time	T_r	-	10	-		
Turn-Off Delay Time	$Td_{(OFF)}$	-	54	-		
Fall Time	T_f	-	26	-		

Notes
1. Pulse test : PW ≦ 300 us duty cycle ≦ 2%.
2. Guaranteed by design, not subject to production testing.