Elektronische Bauelemente

# SSM01N60SL

**1A , 600V , $R_{DS(ON)}$ 8.1Ω**

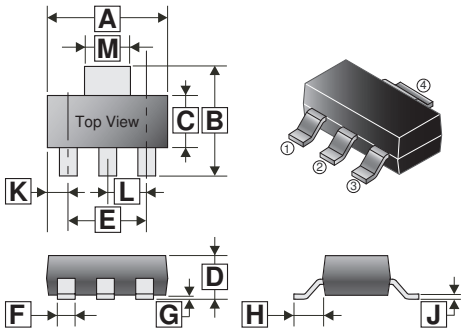
**N-Ch Enhancement Mode Power MOSFET**

RoHS Compliant Product
A suffix of "-C" specifies halogen free

## DESCRIPTION

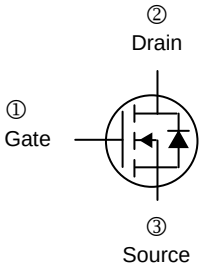
The SSM01N60SL is the highest performance trench N-ch MOSFETs with extreme high cell density , which provide excellent $R_{DS(on)}$ and gate charge for most of the synchronous buck converter applications .

**SOT-223**




## FEATURES

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available




| REF. | Millimeter | | REF. | Millimeter | |
|---|---|---|---|---|---|
| | Min. | Max. | | Min. | Max. |
| A | 5.90 | 6.70 | G | - | 0.18 |
| B | 6.70 | 7.30 | H | 2.00 REF. | |
| C | 3.30 | 3.80 | J | 0.20 | 0.40 |
| D | 1.42 | 1.90 | K | 1.10 REF. | |
| E | 4.45 | 4.75 | L | 2.30 REF. | |
| F | 0.60 | 0.85 | M | 2.80 | 3.20 |

## ABSOLUTE MAXIMUM RATINGS ($T_A$=25℃ unless otherwise specified)

| Parameter | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 600 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±30 | V |
| Continuous Drain Current | $T_C$=25℃ | $I_D$ | 1 | A |
| | $T_C$=100℃ | | 0.6 | A |
| Pulsed Drain Current | | $I_{DM}$ | 4 | A |
| Total Power Dissipation | $T_C$=25℃ | $P_D$ | 22 | W |
| | Derate above 25℃ | | 0.18 | W/℃ |
| Single Pulse Avalanche Energy [1] | | $E_{AS}$ | 52 | mJ |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55~150 | ℃ |
| **Thermal Resistance Rating** | | | | |
| Maximum Thermal Resistance Junction-Ambient | | $R_{\theta JA}$ | 60 | ℃ / W |
| Maximum Thermal Resistance Junction-Case | | $R_{\theta JC}$ | 5.68 | ℃ / W |

Notes:

1. L=30mH,$I_{AS}$=1.74A, $V_{DD}$=110V, $R_G$=25Ω, Starting $T_J$ =25℃

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25℃ unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Teat Conditions |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | 600 | - | - | V | $V_{GS}$=0, $I_D$= 250μA |
| Gate-Threshold Voltage | $V_{GS(th)}$ | 2 | - | 4 | V | $V_{DS}$=$V_{GS}$, $I_D$=250μA |
| Gate-Source Leakage Current | $I_{GSS}$ | - | - | ±100 | nA | $V_{GS}$= ±30V, $V_{DS}$=0 |
| Drain-Source Leakage Current | $I_{DSS}$ | - | - | 1 | μA | $V_{DS}$=600V, $V_{GS}$=0 |
| Static Drain-Source On-Resistance | $R_{DS(ON)}$ | - | 6.8 | 8.1 | Ω | $V_{GS}$=10V, $I_D$=0.5A |
| Total Gate Charge [1.2] | $Q_g$ | - | 3.37 | - | nC | $I_D$=1A<br>$V_{DS}$=480V<br>$V_{GS}$=10V |
| Gate-Source Charge [1.2] | $Q_{gs}$ | - | 1.16 | - | | |
| Gate-Drain Change [1.2] | $Q_{gd}$ | - | 1.04 | - | | |
| Turn-on Delay Time [1.2] | $T_{d(on)}$ | - | 6.1 | - | nS | $V_{DD}$=300V<br>$I_D$=1A<br>$R_G$=25 Ω |
| Rise Time [1.2] | $T_r$ | - | 11.9 | - | | |
| Turn-off Delay Time [1.2] | $T_{d(off)}$ | - | 8.3 | - | | |
| Fall Time [1.2] | $T_f$ | - | 15.3 | - | | |
| Input Capacitance | $C_{iss}$ | - | 139 | - | pF | $V_{GS}$ =0<br>$V_{DS}$=25V<br>f =1.0MHz |
| Output Capacitance | $C_{oss}$ | - | 23.4 | - | | |
| Reverse Transfer Capacitance | $C_{rss}$ | - | 0.6 | - | | |
| **Source-Drain Diode** | | | | | | |
| Diode Forward Voltage | $V_{SD}$ | - | - | 1.5 | V | $I_S$=1A, $V_{GS}$=0 |
| Continuous Source Current | $I_S$ | - | - | 1 | A | Integral Reverse P-N Junction Diode in the MOSFET |
| Pulsed Source Current | $I_{SM}$ | - | - | 4 | A | |
| Reverse Recovery Time | $T_{rr}$ | - | 190 | - | ns | $I_S$=1A,$V_{GS}$=0,<br>$dI_F/dt$=100A/μS |
| Reverse Recovery Charge | $Q_{rr}$ | - | 0.53 | - | μC | |

Notes:
1. Pulse Test: Pulse width ≦300μS, Duty cycle≦2%
2. Essentially independent of operating temperature.

## CHARACTERISTIC CURVES

Figure 1. On-Region Characteristics

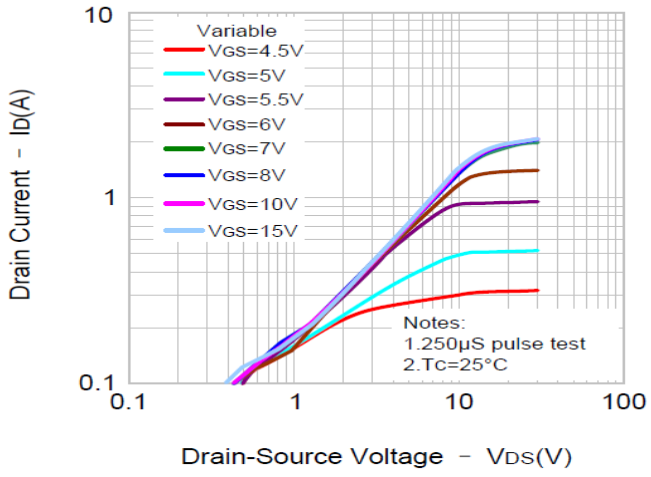



Figure 2. Transfer Characteristics

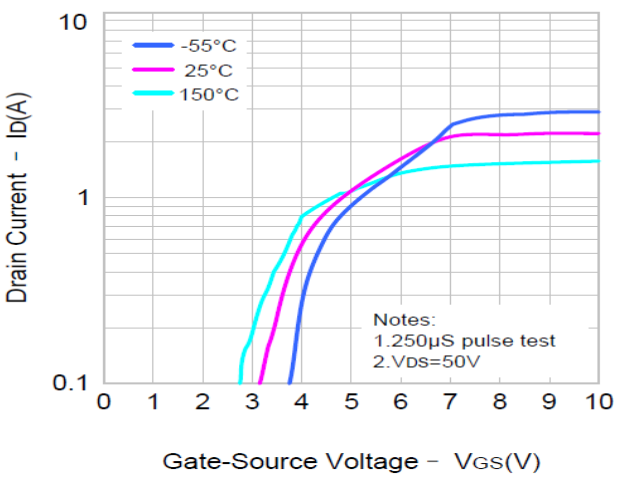



Figure 3. On-Resitance Variation vs. Drain Current and Gate Voltage

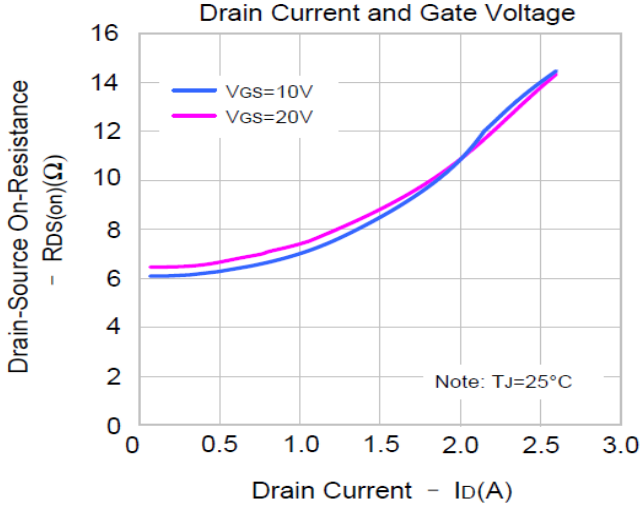



Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

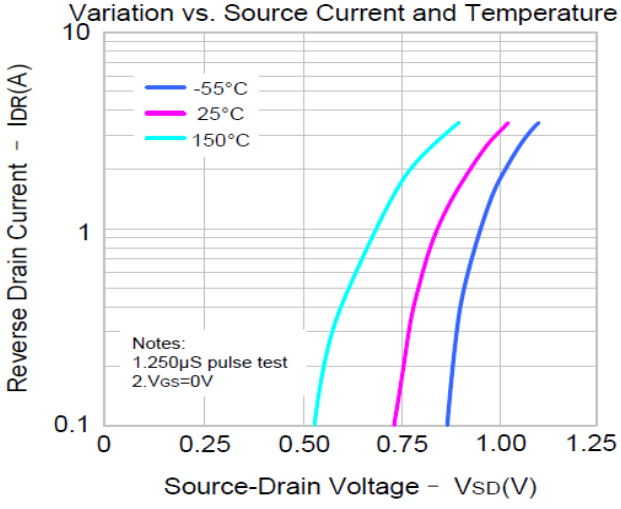



Figure 5. Capacitance Characteristics

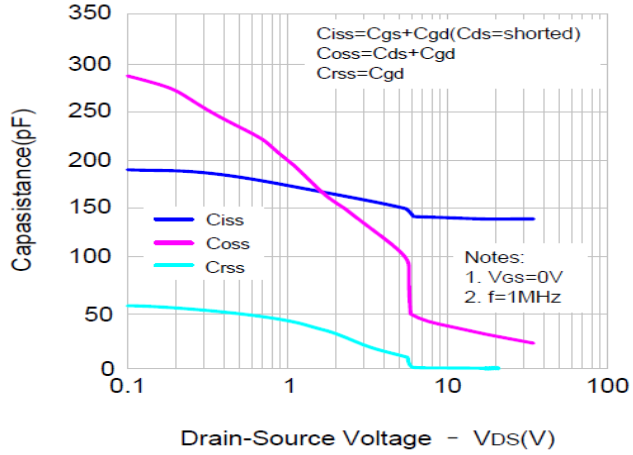
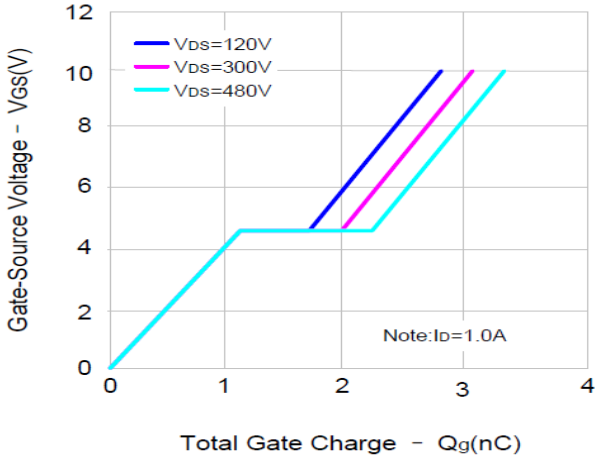



Figure 6. Gate Charge Characteristics



## CHARACTERISTIC CURVES

Figure 7. Breakdown Voltage Variation vs. Temperature

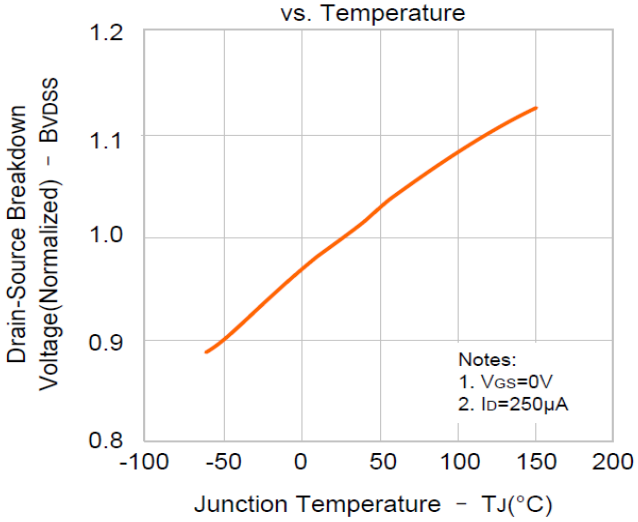



Figure 8. On-resistance Variation vs. Temperature

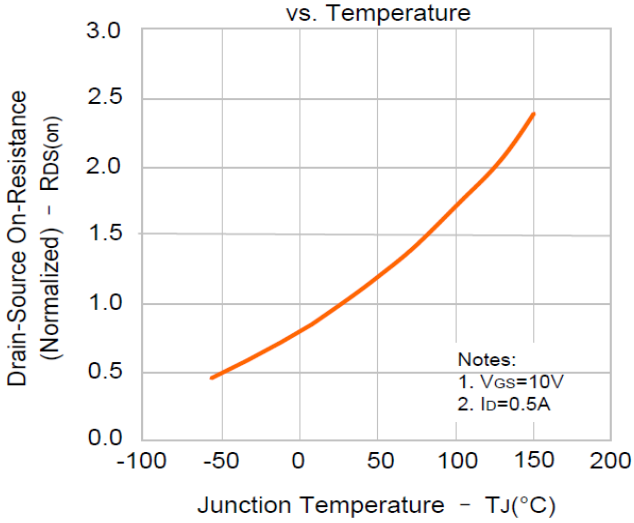



Figure 9-4. Max. Safe Operating Area

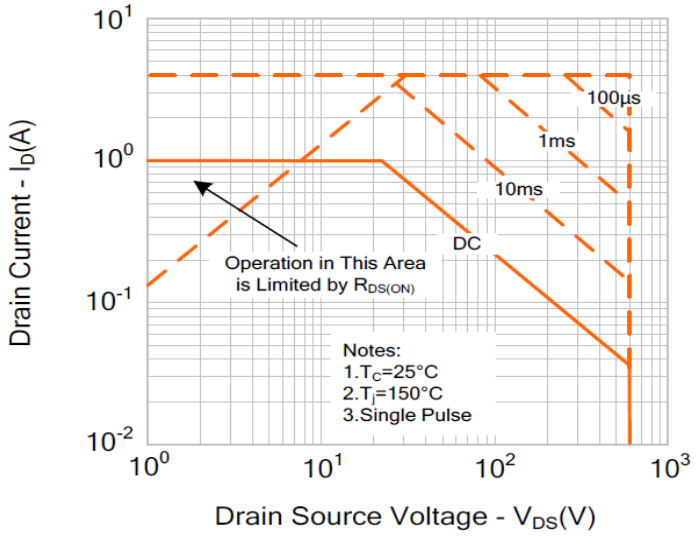
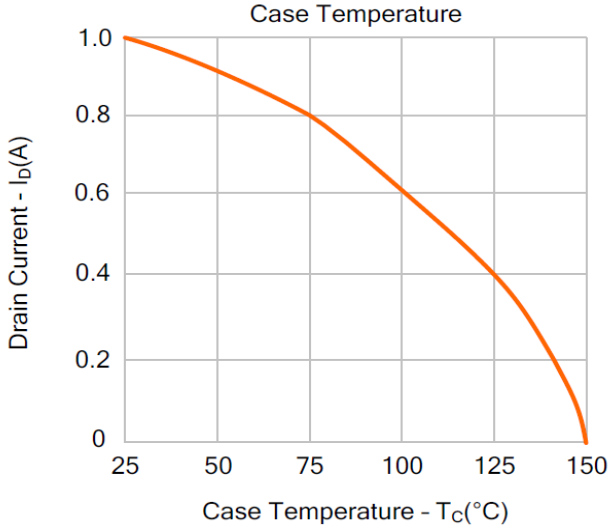
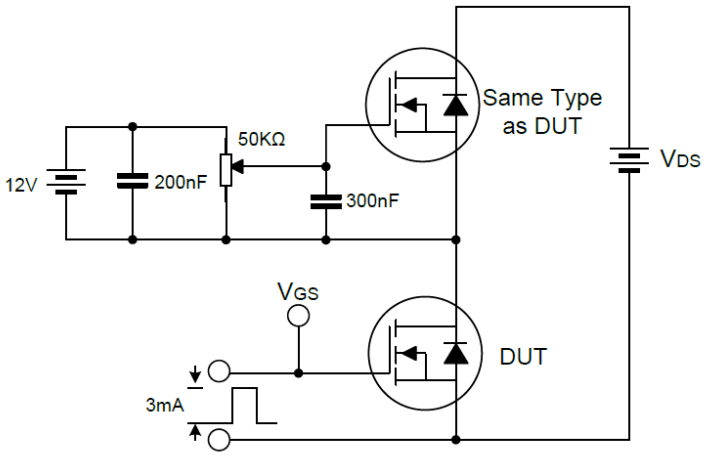


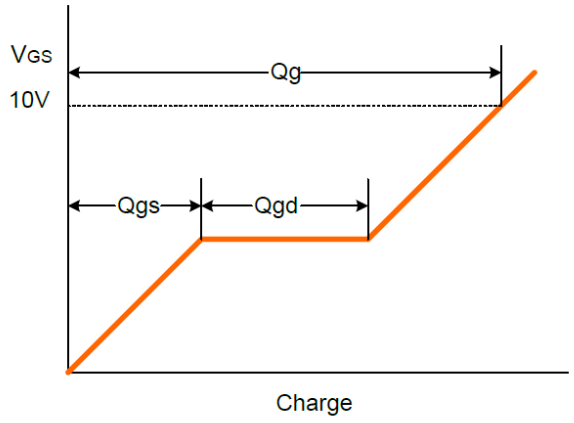

Figure 10. Maximum Drain Current vs. Case Temperature



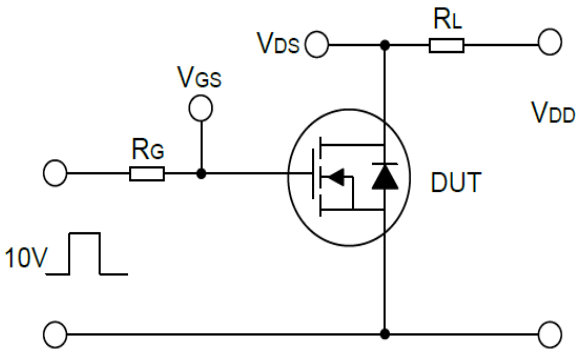
## TYPICAL TEST CURVES

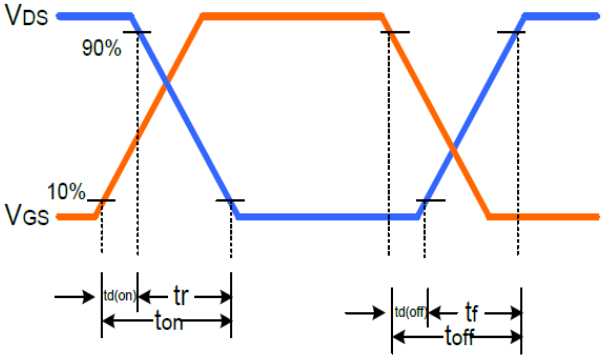
Gate Charge Test Circuit & Waveform



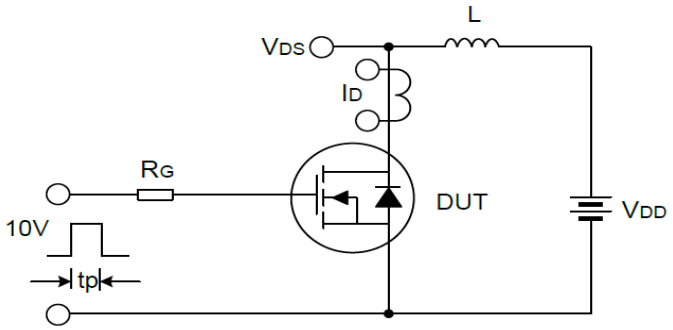




Resistive Switching Test Circuit & Waveform




Unclamped Inductive Switching Test Circuit & Waveform




$$E_{AS} = \frac{1}{2} LI_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$