Elektronische Bauelemente

SST3585S

4.3A, 20V, $R_{DS(ON)}$ 37mΩ
-3.1A, -20V, $R_{DS(ON)}$ 75mΩ
N And P-Channel Enhancement Mode Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

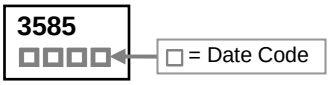
The SST3585S is the highest performance trench N-ch MOSFETs with extreme high cell density , which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The SST3585S meet the RoHS and Green Product requirement with full function reliability approved.

FEATURES

- Low Gate Charge
- Low On-resistance

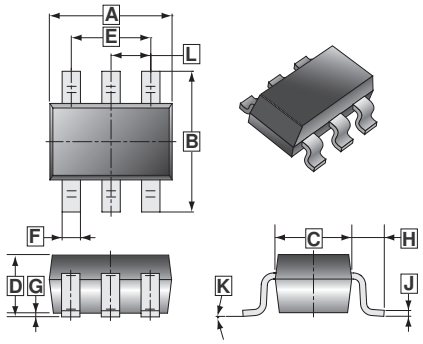
MARKING



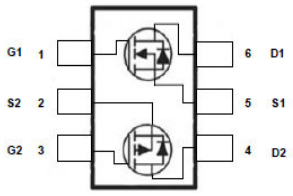
PACKAGE INFORMATION

Package	MPQ	Leader Size
SOT-26	3K	7 inch

SOT-26



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	0	0.10
B	2.60	3.00	H	0.60 REF.	
C	1.40	1.80	J	0.12 REF.	
D	1.30 MAX.		K	0°	10°
E	1.90 REF.		L	0.95 REF.	
F	0.25	0.50			



ABSOLUTE MAXIMUM RATINGS (T_A=25℃ unless otherwise specified)

Parameter		Symbol	Rating		Unit
			N-Channel	P-Channel	
Drain-Source Voltage		V_{DS}	20	-20	V
Gate-Source Voltage		V_{GS}	±12	±12	V
Continuous Drain Current [1] @V_{GS}=4.5V	T_A= 25℃	I_D	4.3	-3.1	A
	T_A= 70℃		3.4	-2.5	
Pulsed Drain Current [3]		I_{DM}	17.2	-12.4	A
Power Dissipation		P_D	1.14		W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150		℃
Thermal Date					
Maximum Thermal Resistance from Junction to Ambient [1]		$R_{\theta JA}$	110		℃ / W
Maximum Thermal Resistance from Junction to Ambient [2]			180		

ELECTRICAL CHARACTERISTICS (T_J=25℃ unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Condition
Static							
Drain-Source Breakdown Voltage	N-Ch	BV_{DSS}	20	-	-	V	V_{GS}=0, I_D=250μA
	P-Ch		-20	-	-		V_{GS}=0, I_D= -250μA
Breakdown Voltage Temp. Coefficient	N-Ch	$\triangle BV_{DSS}/\triangle T_J$	-	0.018	-	V/℃	Reference to 25℃, I_D=1mA
	P-Ch		-	-0.01	-		Reference to 25℃, I_D= -1mA
Gate-Threshold Voltage	N-Ch	$V_{GS(th)}$	0.5	-	1.2	V	V_{DS}=V_{GS}, I_D=250μA
	P-Ch		-0.5	-	-1.2		V_{DS}=V_{GS}, I_D= -250μA
Forward Transfer conductance	N-Ch	g_{fs}	-	20	-	S	V_{DS}=5V, I_D=4A
	P-Ch		-	9	-		V_{DS}= -5V, I_D= -3A
Gate-Source Leakage Current	N-Ch	I_{GSS}	-	-	±100	nA	V_{GS}= ±12V
	P-Ch		-	-	±100		V_{GS}= ±12V
Drain-Source Leakage Current	N-Ch	I_{DSS}	-	-	1	μA	V_{DS}=16V, V_{GS}=0, T_J=25℃
	P-Ch		-	-	-1		V_{DS}= -16V, V_{GS}=0, T_J=25℃
	N-Ch		-	-	5		V_{DS}=16V, V_{GS}=0, T_J=55℃
	P-Ch		-	-	-5		V_{DS}= -16V, V_{GS}=0, T_J=55℃
Drain-Source On-Resistance [4]	N-Ch	$R_{DS(ON)}$	-	-	37	mΩ	V_{GS}=4.5V, I_D=4A
	P-Ch		-	-	75		V_{GS}= -4.5V, I_D= -3A
	N-Ch		-	-	45		V_{GS}=2.5V, I_D=3A
	P-Ch		-	-	105		V_{GS}= -2.5V, I_D= -2A
Total Gate Charge	N-Ch	Q_g	-	8.6	-	nC	N-Channel V_{DS}=15V, V_{GS}=4.5V, I_D=4A P-Channel V_{DS}= -15V, V_{GS}= -4.5V, I_D= -3A
	P-Ch		-	9.7	-		
Gate-Source Charge	N-Ch	Q_{gs}	-	1.37	-		
	P-Ch		-	2.05	-		
Gate-Drain Charge	N-Ch	Q_{gd}	-	2.3	-		
	P-Ch		-	2.43	-		
Turn-on Delay Time[1]	N-Ch	$T_{d(on)}$	-	5.2	-	nS	N-Channel V_{DS}=10V,V_{GS}=4.5V,I_D=4A R_G=3.3Ω,R_D=2.5Ω P-Channel V_{DS}= -10V, V_{GS}= -4.5V, I_D= -3A R_G=3.3Ω, R_D=3.33Ω
	P-Ch		-	4.8	-		
Rise Time	N-Ch	T_r	-	34	-		
	P-Ch		-	9.6	-		
Turn-off Delay Time	N-Ch	$T_{d(off)}$	-	23	-		
	P-Ch		-	52	-		
Fall Time	N-Ch	T_f	-	9.2	-		
	P-Ch		-	8.4	-		
Input Capacitance	N-Ch	C_{iss}	-	635	-	pF	N-Channel V_{GS}=0, V_{DS}=15V, f=1.0MHz P-Channel V_{GS}=0, V_{DS}= -15V, f=1MHz
	P-Ch		-	686	-		
Output Capacitance	N-Ch	C_{oss}	-	70	-		
	P-Ch		-	90.8	-		
Reverse Transfer Capacitance	N-Ch	C_{rss}	-	63	-		
	P-Ch		-	80.4	-		

ELECTRICAL CHARACTERISTICS (T_J=25℃ unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Condition
Source-Drain Diode							
Continuous Source Current [1]	N-Ch	I_S	-	-	4.3	A	
	P-Ch		-	-	-3.1		
Pulsed Source Current [3]	N-Ch	I_{SM}	-	-	17.2	A	
	P-Ch		-	-	-12.4		
Forward On Voltage [4]	N-Ch	V_{SD}	-	0.7	1.2	V	I_S=1A, V_{GS}=0
	P-Ch		-	-0.7	-1.2		I_S= -1A, V_{GS}=0
Reverse Recovery Time	N-Ch	T_{rr}	-	7.5	-	nS	I_S=4A, V_{GS}=0, dI/dt=100A/μs
	P-Ch		-	8.4	-		I_S= -3A, V_{GS}=0 ,dI/dt=100A/μs
Reverse Recovery Charge	N-Ch	Q_{rr}	-	2.1	-	nC	I_S=4A, V_{GS}=0 ,dI/dt=100A/μs
	P-Ch		-	3.3	-		I_S= -3A, V_{GS}=0 ,dI/dt=100A/μs

Notes:

1. Surface mounted on a 1 inch^2 FR-4 board with 2OZ copper. t≦5s.
2. Surface mounted on FR4 Board using the minimum recommended pad size.
3. The power dissipation is limited by 150℃ junction temperature, Pw ≤ 300μs, Duty cycle ≤ 1%.
4. The data tested by pulsed , pulse width ≦ 300μs , duty cycle ≦ 2%

CHARACTERISTICS CURVE (N-Channel)

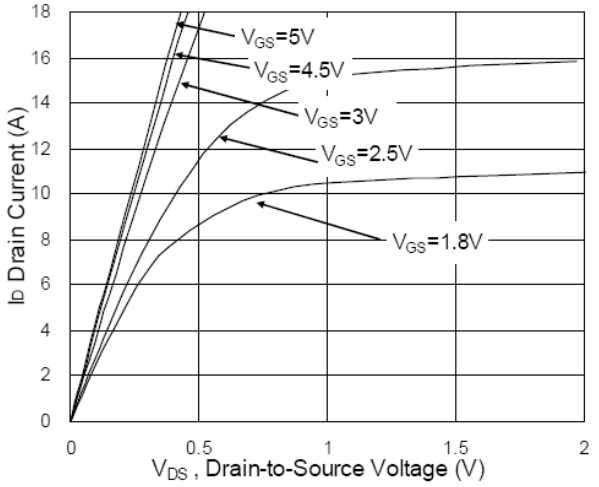


Fig.1 Typical Output Characteristics

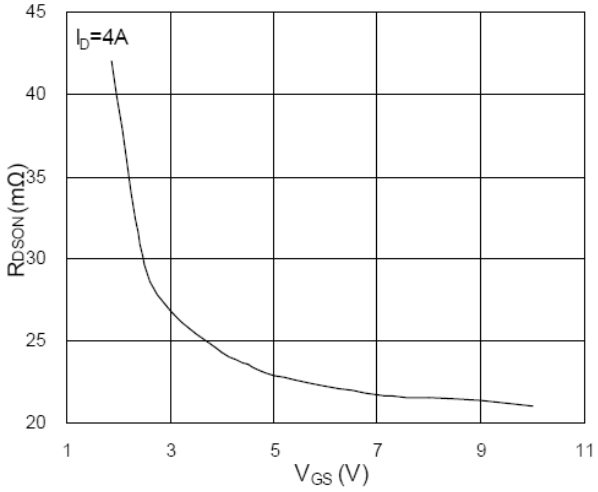


Fig.2 On-Resistance vs. Gate-Source

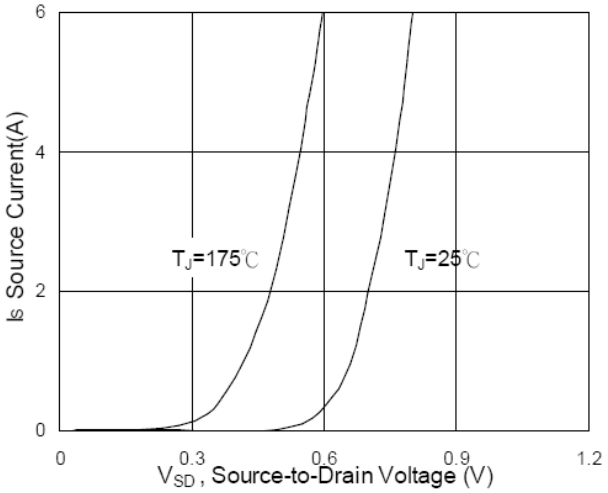


Fig.3 Forward Characteristics Of Reverse

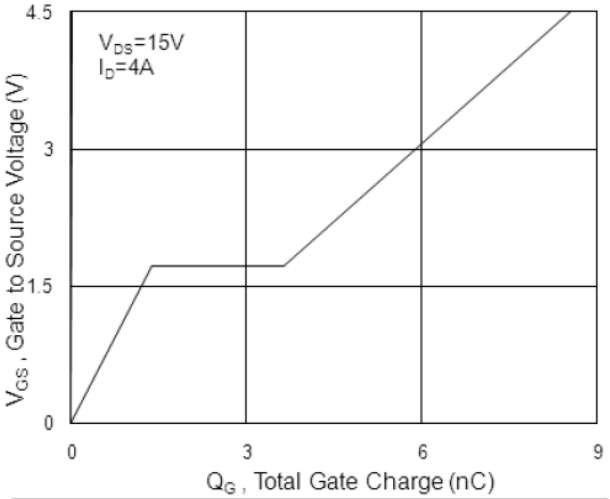


Fig.4 Gate-Charge Characteristics

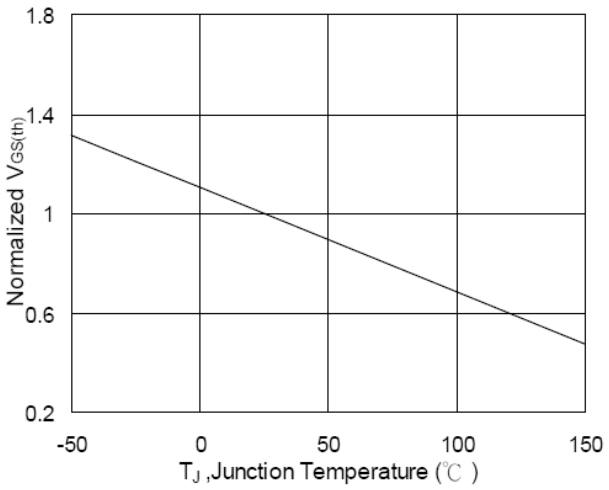


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

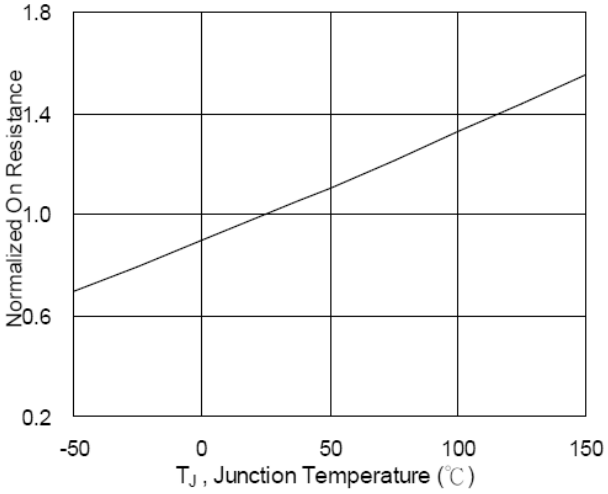


Fig.6 Normalized R_{DSON} vs. T_J

CHARACTERISTICS CURVE (N-Channel)

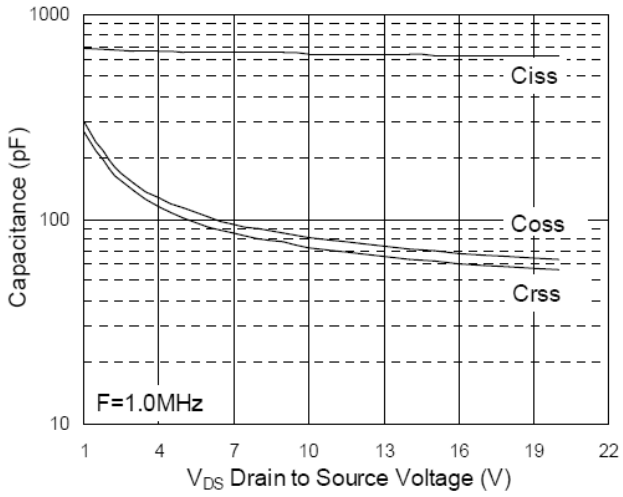


Fig.7 Capacitance

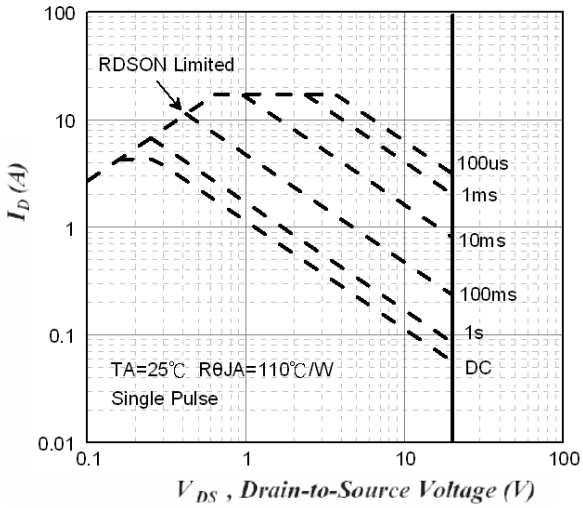


Fig.8 Safe Operating Area

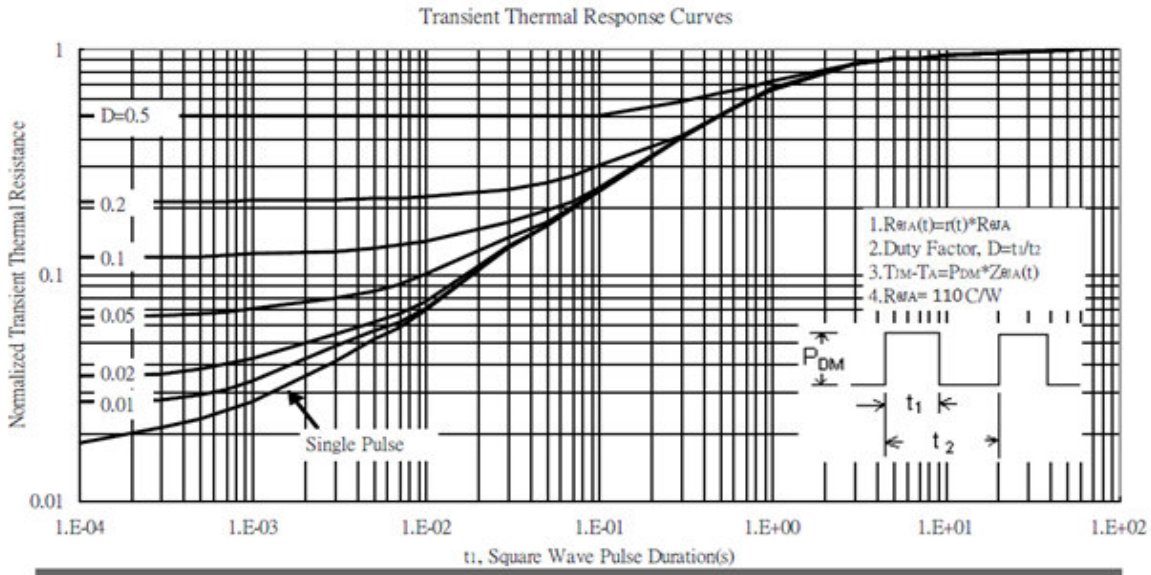


Fig.9 Normalized Maximum Transient Thermal Impedance

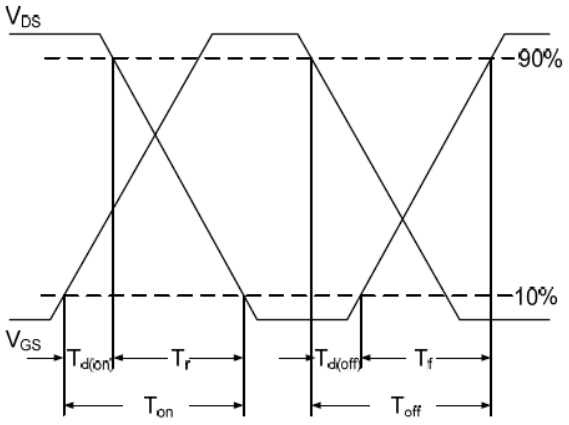


Fig.10 Switching Time Waveform

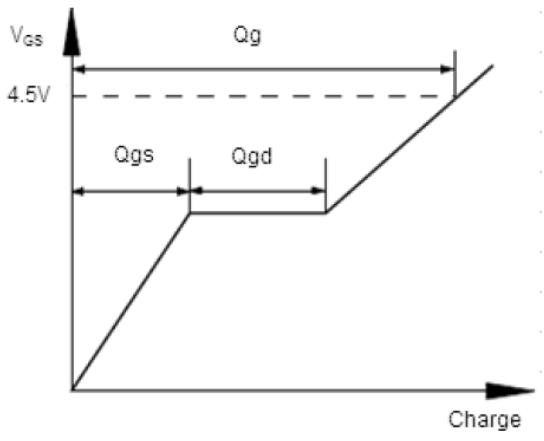


Fig.11 Gate Charge Waveform

CHARACTERISTICS CURVE (P-Channel)

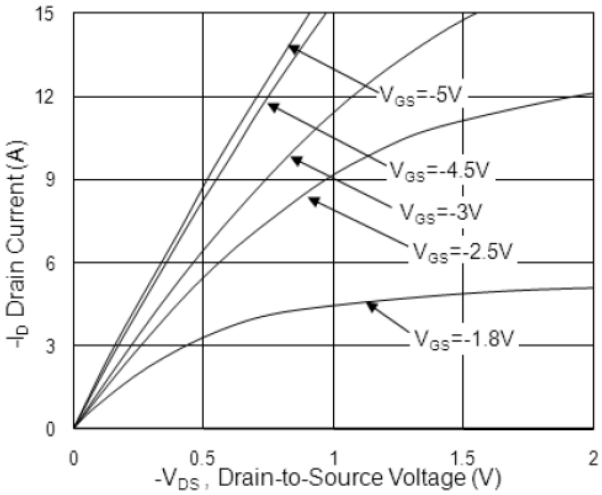


Fig.1 Typical Output Characteristics

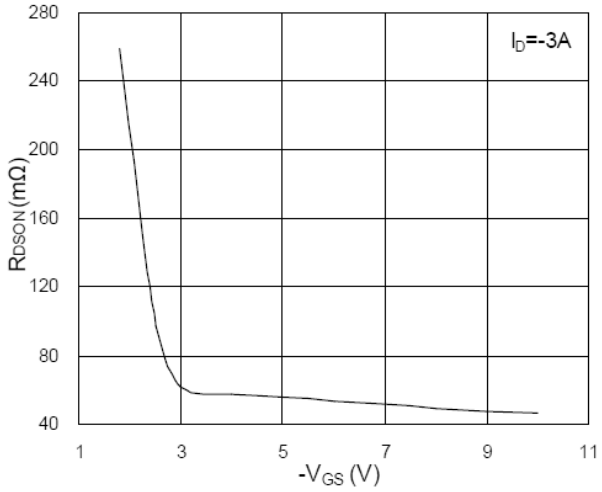
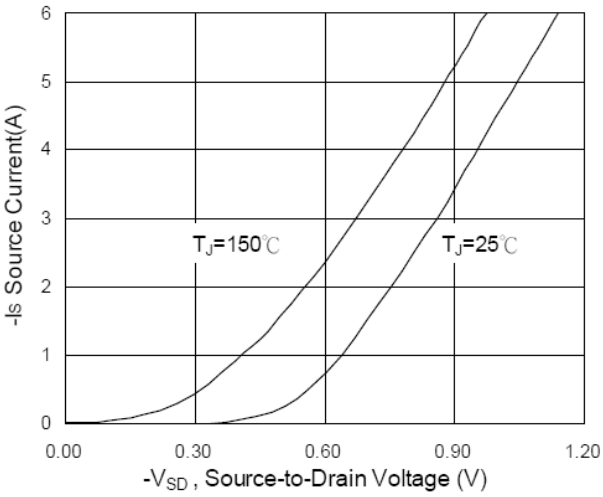


Fig.2 On-Resistance vs. Gate-Source



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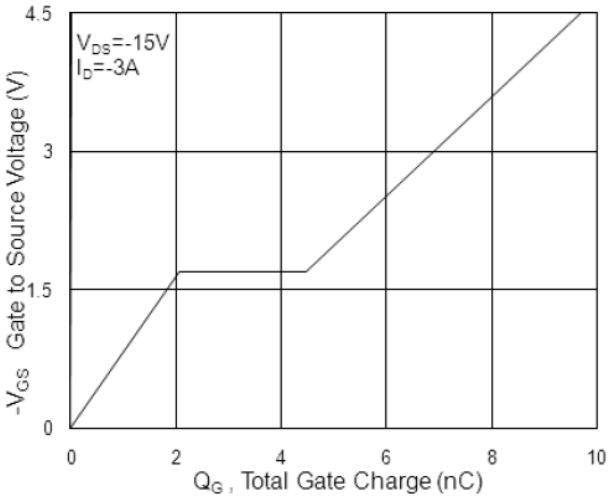


Fig.4 Gate-Charge Characteristics

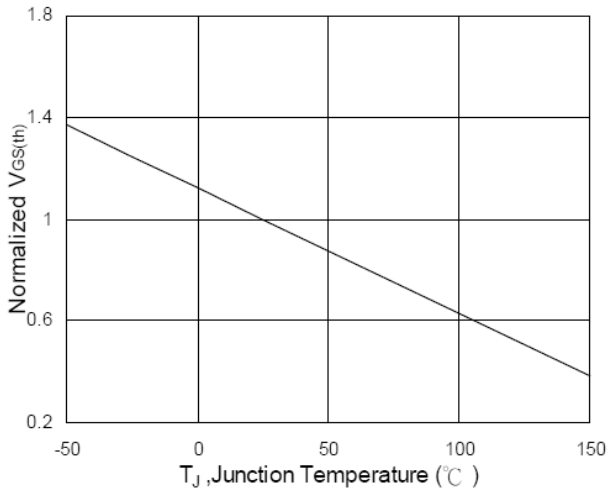


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

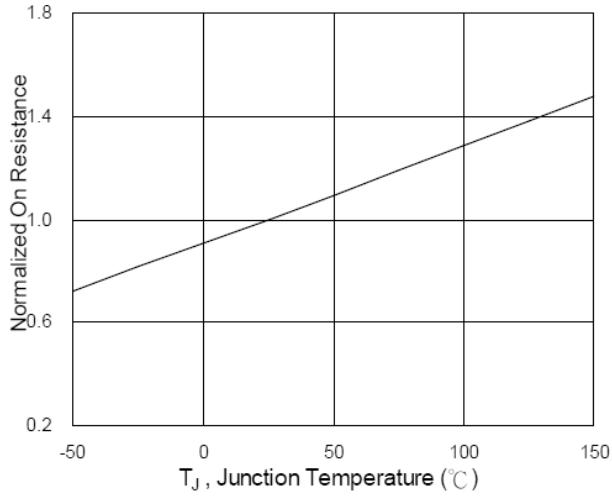


Fig.6 Normalized R_{DSON} vs. T_J

CHARACTERISTICS CURVE (P-Channel)

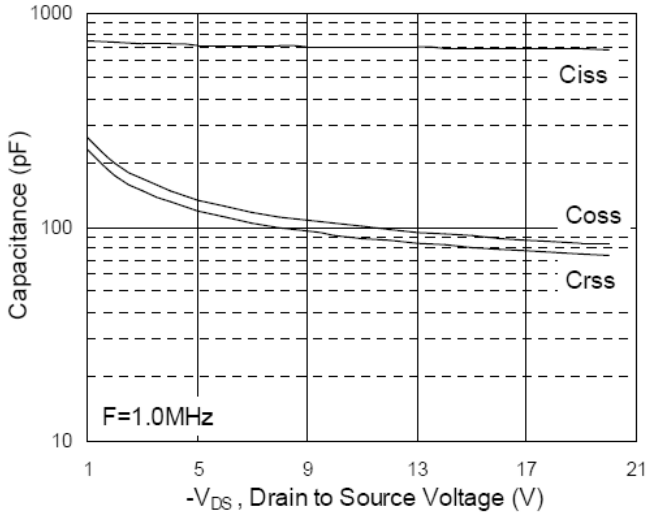
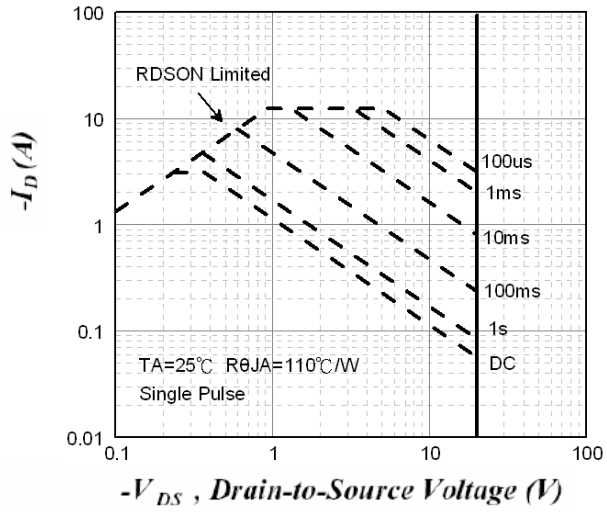


Fig.7 Capacitance



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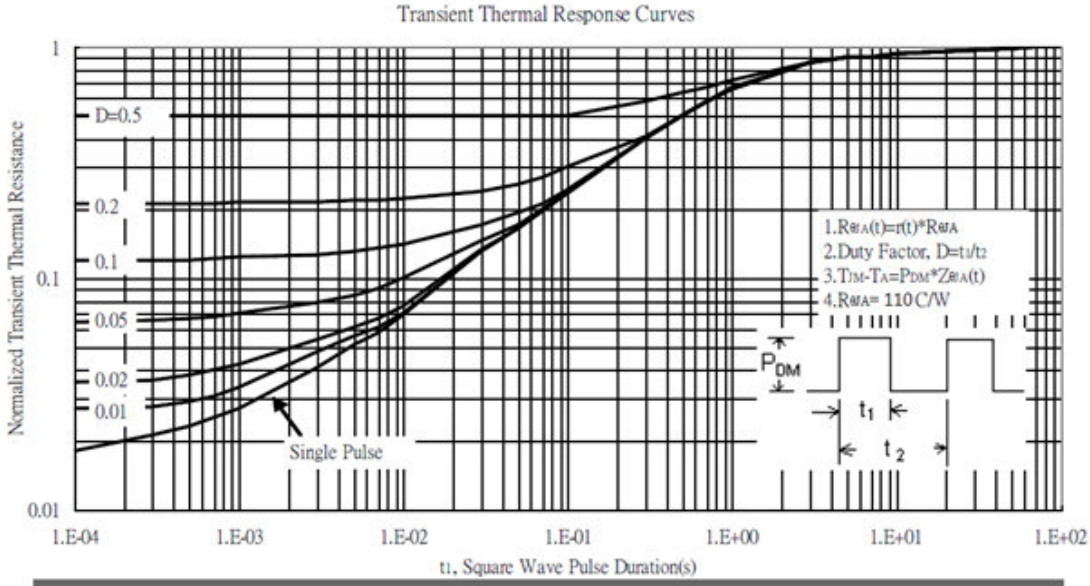

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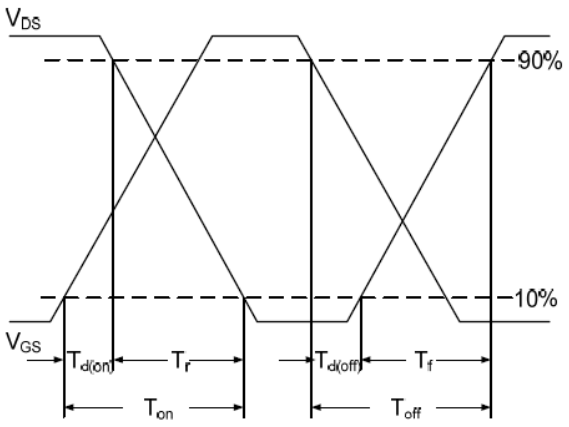

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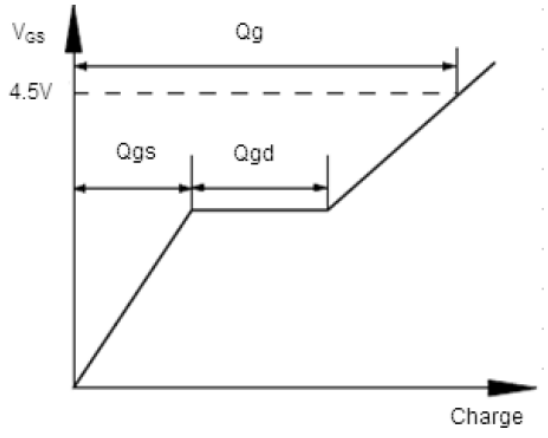

Fig.11 Gate Charge Waveform