

RoHS Compliant Product
A Suffix of "-C" specifies halogen & lead-free

FEATURES

- Low on-resistance
- Fast switching Speed
- Low-voltage drive
- Easily designed drive circuits
- ESD protected: 1500V

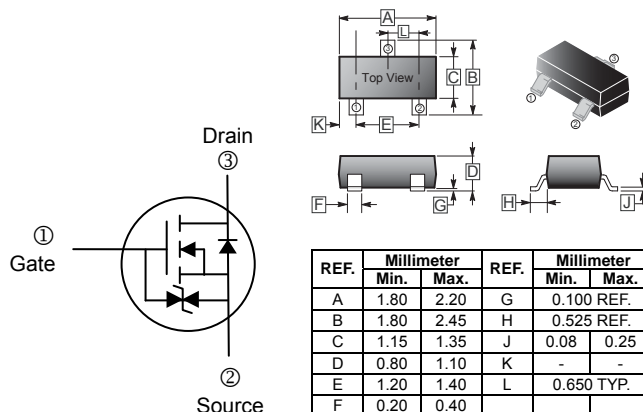
MARKING

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PACKAGE INFORMATION

Package	MPQ	Leader Size
SOT-323	3K	7' inch

SOT-323



MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

PARAMETER	SYMBOL	RATING	UNIT
Drain – Source Voltage	V _{DSS}	60	V
Continuous Gate – Source Voltage	V _{GSS}	±20	V
Continuous Drain Current	I _D	115	mA
Pulsed Drain Current	I _{DP} ¹	800	mA
Continuous Reverse Drain Current	I _{DR}	115	mA
Pulsed Reverse Drain Current	I _{DRP} ¹	800	mA
Total Power Dissipation	P _D ²	225	mW
Channel & Storage Temperature Range	T _{CH} , T _{STG}	150, -55~150	°C

Note:

1. P_w ≤ 10μS, Duty cycle ≤ 1%
2. When mounted on a 1x0.75x0.062 inch glass epoxy board

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified, per element)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
OFF CHARACTERISTICS ²						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	60	-	-	V	V _{GS} =0V, I _D =10μA
Zero Gate Voltage Drain Current	I _{DSS}	-	-	1.0	μA	V _{DS} =60V, V _{GS} =0V
Gate-Source Leakage	I _{GSS}	-	-	±10	μA	V _{DS} =0V, V _{GS} =±20V
ON CHARACTERISTICS ²						
Gate-Threshold Voltage	V _{GS(TH)}	1	1.85	2.5	V	V _{DS} = V _{GS} , I _D =250μA
Static Drain-Source On Resistance	R _{DS(ON)}	-	-	7.5	Ω	V _{GS} =10V, I _D =0.5A
		-	-	7.5		V _{GS} =5V, I _D =0.05A
Forward Transfer Admittance	g _{Fs} [*]	80	-	-	ms	V _{DS} =10V, I _D =0.2A
DYNAMIC CHARACTERISTICS						
Input Capacitance	C _{ISS}	-	25	50	pF	V _{DS} =25V
Output Capacitance	C _{OSS}	-	10	25		V _{GS} =0V
Reverse Transfer Capacitance	C _{RSS}	-	3.0	5		f=1MHz
SWITCHING CHARACTERISTICS						
Turn-on Delay Time	T _{d(ON)} [*]	-	12	20	nS	V _{DD} =30V, I _D =0.2A
Turn-off Delay Time	T _{d(OFF)} [*]	-	20	30		R _L =150Ω, V _{GS} =10V, R _G =10Ω

* P_w ≤ 300μS, Duty cycle ≤ 1%

CHARACTERISTIC CURVES

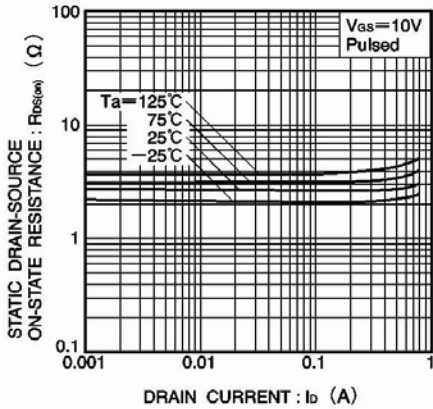


Fig.4 Static drain-source on-state resistance vs. drain current (I)

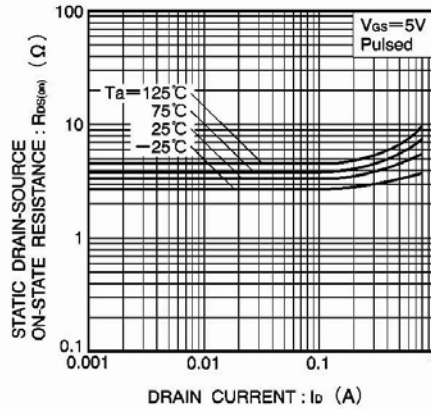


Fig.5 Static drain-source on-state resistance vs. drain current (II)

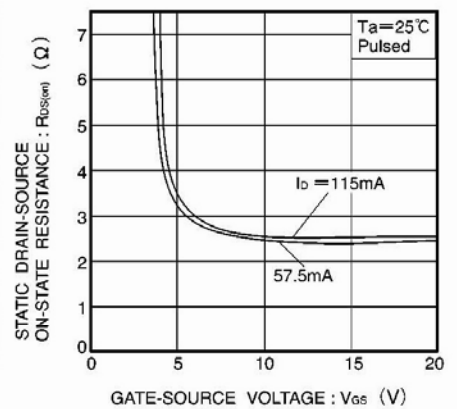


Fig.6 Static drain-source on-state resistance vs. gate-source voltage

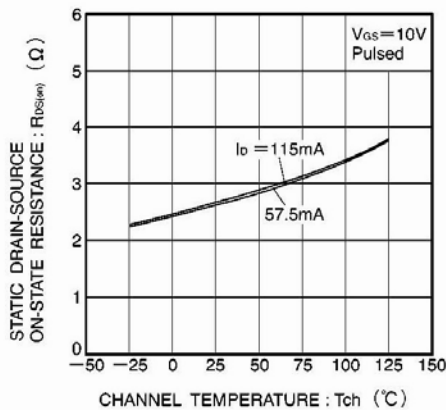


Fig.7 Static drain-source on-state resistance vs. channel temperature

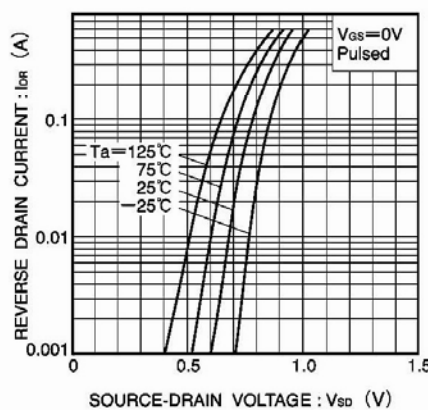


Fig.8 Reverse drain current vs. source-drain voltage (I)

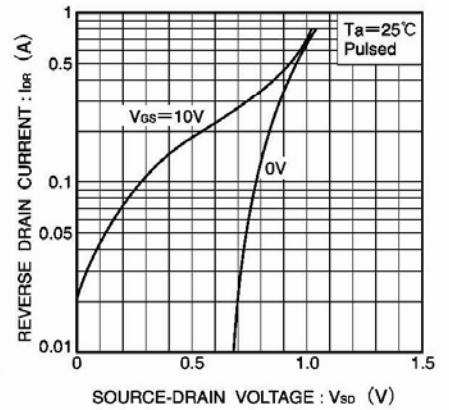


Fig.9 Reverse drain current vs. source-drain voltage (II)

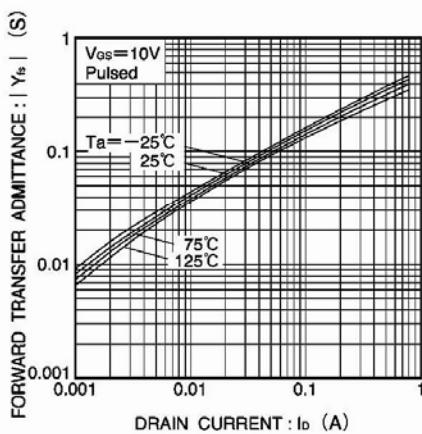


Fig.10 Forward transfer admittance vs. drain current

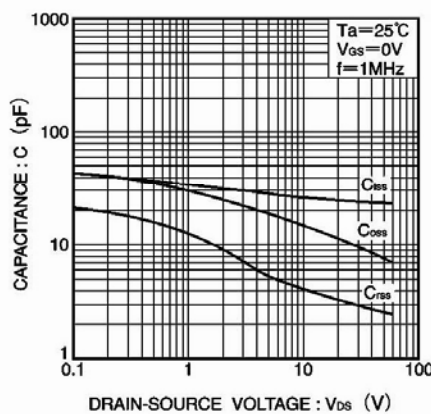


Fig.11 Typical capacitance vs. drain-source voltage

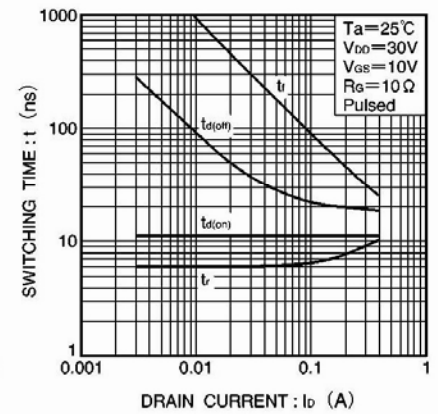


Fig.12 Switching characteristics (See Figures 13 and 14 for the measurement circuit and resultant waveforms)