Elektronische Bauelemente

SSPR48N10-C

48A, 100V, $R_{DS(ON)}$ 9.8mΩ

N-Channel Enhancement Mode Power MOSFET

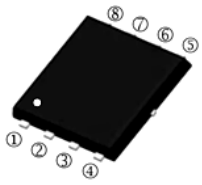
RoHS Compliant Product

A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

These N-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency fast switching application.

SPR-8PP



FEATURES

- Improved dv/dt capability
- Fast switching
- Green Device Available

APPLICATION

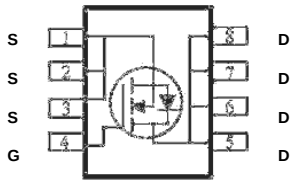
- Networking
- Load Switch
- LED applications

MARKING

NM9P8

PACKAGE INFORMATION

Package	MPQ	Leader Size
SPR-8PP	3K	13 inch



ORDER INFORMATION

Part Number	Type
SSPR48N10-C	Lead (Pb)-free and Halogen-free

ABSOLUTE MAXIMUM RATINGS (T_C=25℃ unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25℃	I_D	48	A
	T_C=100℃		30	
Pulsed Drain Current [1]		I_{DM}	88	A
Power Dissipation	T_C=25℃	P_D	26.3	W
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-50~150	℃
Thermal Resistance Ratings				
Thermal Resistance Junction-Case		$R_{\theta JC}$	4.75	℃/W

ELECTRICAL CHARACTERISTICS (T_J=25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV_{DSS}	100	-	-	V	V_{GS}=0V, I_D=250μA
Gate-Threshold Voltage	$V_{GS(th)}$	1.0	-	3	V	V_{DS}=V_{GS}, I_D=250μA
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}=±20V, V_{DS}=0V
Drain-Source Leakage Current	I_{DSS}	-	-	1	μA	V_{DS}=80V, V_{GS}=0V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	-	-	9.8	mΩ	V_{GS}=10V, I_D=15A
		-	-	14		V_{GS}=4.5V, I_D=10A
Gate Resistance	R_g	-	0.8	-	Ω	V_{DS}=V_{GS}=0V, f=1MHz
Forward Transconductance	g_{fs}	-	22.3	-	S	V_{GS}=10V, I_D=5A
Total Gate Charge	Q_g	-	39.9	-	nC	V_{DS}=50V V_{GS}=10V I_D=20A
Gate-Source Charge	Q_{gs}	-	8.92	-		
Gate-Drain Change	Q_{gd}	-	10.4	-		
Turn-on Delay Time	$T_{d(on)}$	-	9.2	-	nS	V_{DS}=50V V_{GS}=10V I_D=1A R_G=6Ω
Rise Time	T_r	-	17.6	-		
Turn-off Delay Time	$T_{d(off)}$	-	32.2	-		
Fall Time	T_f	-	69.9	-		
Input Capacitance	C_{iss}	-	1910	-	pF	V_{DS}=50V V_{GS}=0V f=1MHz
Output Capacitance	C_{oss}	-	506	-		
Reverse Transfer Capacitance	C_{rss}	-	36	-		
Source-Drain Diode						
Reverse Recovery Time	t_{rr}	-	37	-	A	I_F=10A, V_R=50V, dI/dt=100A/μs
Reverse Recovery Charge	Q_{rr}	-	35	-		
Diode Forward Voltage	V_{SD}	-	-	1.1	V	I_S=10A, V_{GS}=0V

Notes:
1. Repetitive Rating：Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width≦300μs , duty cycle≦2%.
3. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS

FIG. 1- On-Resistance vs. I_D

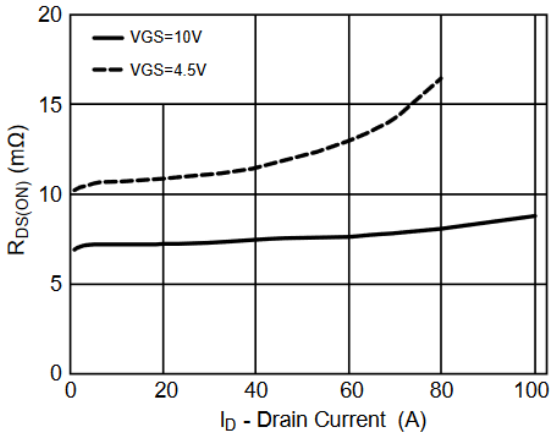


FIG. 2- Gate Threshold Voltage

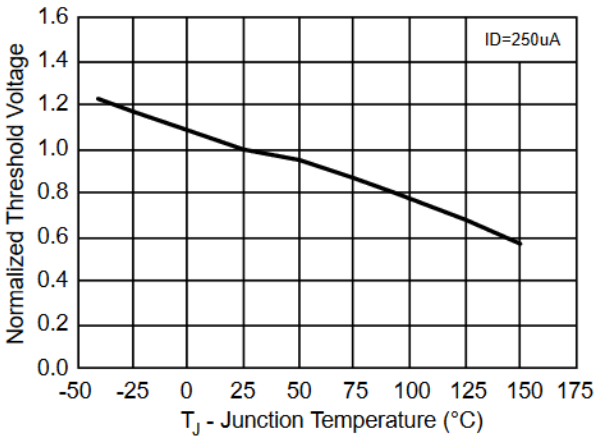


FIG. 3- Gate Charge Characteristics

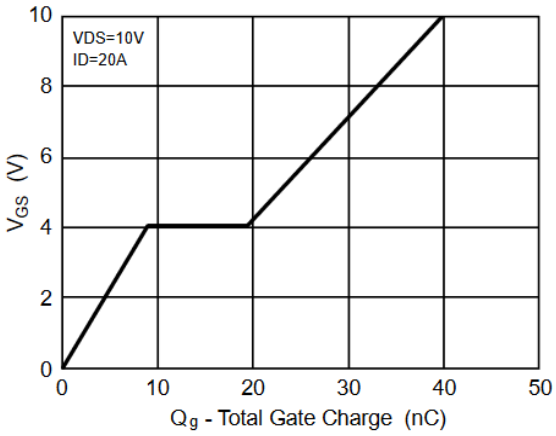


FIG. 4- Drain Current

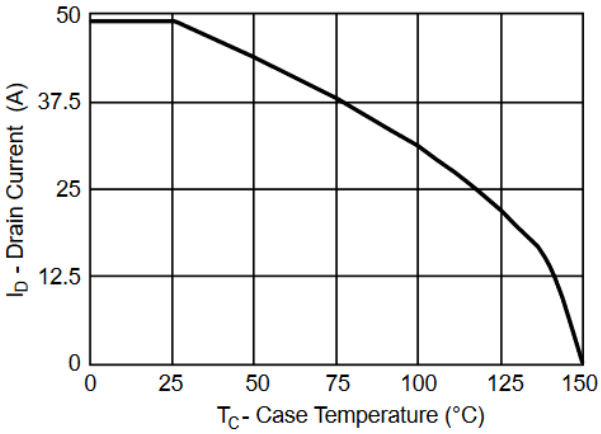


FIG. 5- Safe Operating Area

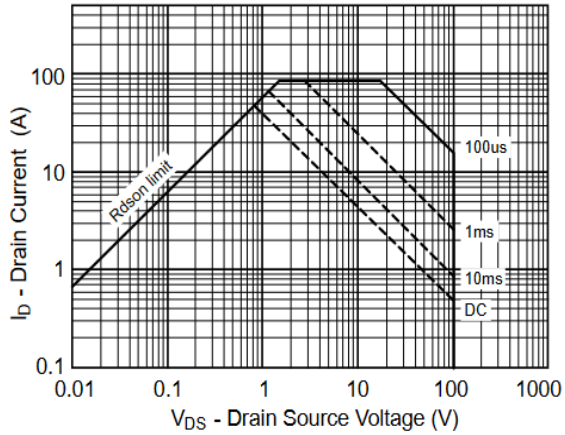
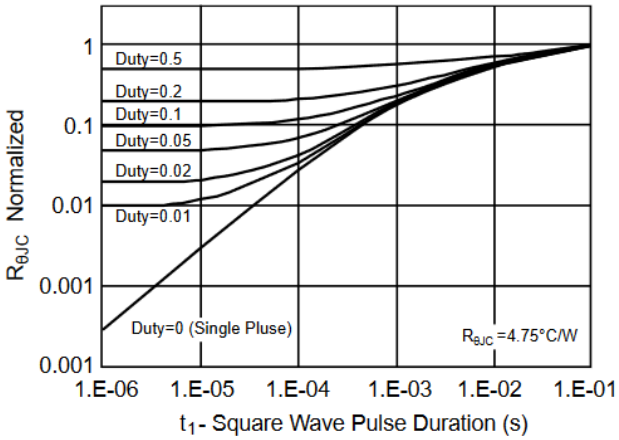
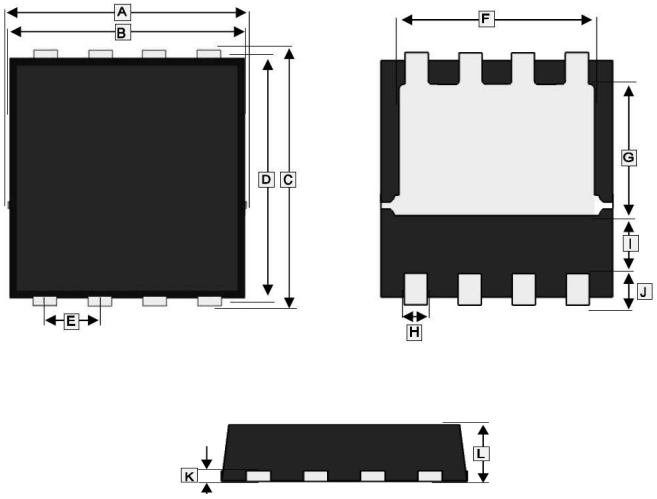


FIG. 6- $R_{\theta JC}$ Transient Thermal Impedance



PACKAGE OUTLINE DIMENSIONS

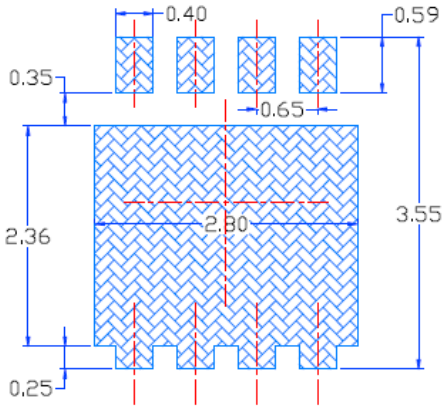
SPR-8PP



REF.	Millimeter	
	Min.	Max.
A	3.00	3.45
B	3.00	3.25
C	3.05	3.50
D	2.90	3.20
E	0.65 BSC.	
F	2.29	2.65
G	1.35	1.98
H	0.20	0.40
I	0.57	0.87
J	0.30	0.60
K	0.10	0.25
L	0.60	0.90

MOUNTING PAD LAYOUT

SPR-8PP



*Dimensions in millimeters