Elektronische Bauelemente

SID02N65SL

2A , 650V , $R_{DS(ON)}$ 4.8Ω

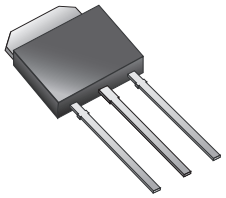
N-Ch Enhancement Mode Power MOSFET

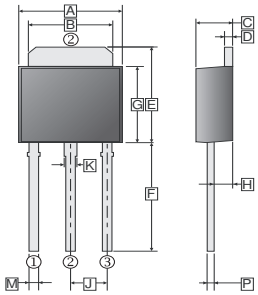
RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

The SID02N65SL is the highest performance trench N-ch MOSFETs with extreme high cell density , which provide excellent $R_{DS(on)}$ and gate charge for most of the synchronous buck converter applications .

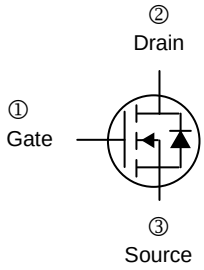
TO-251





FEATURES

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.35	6.80	G	5.40	6.25
B	4.90	5.50	H	0.85	1.50
C	2.15	2.40	J	2.30	
D	0.45	0.90	K	0.60	1.05
E	6.50	7.50	M	0.50	0.90
F	7.20	9.65	P	0.45	0.62

ABSOLUTE MAXIMUM RATINGS (T_A=25℃ unless otherwise specified)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DS}	650	V
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current	T_C=25℃	I_D	2	A
	T_C=100℃		1.3	A
Pulsed Drain Current		I_{DM}	8	A
Total Power Dissipation	T_C=25℃	P_D	38	W
	Derate above 25℃		0.3	
Single Pulse Avalanche Energy [1]		E_{AS}	100	mJ
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150	℃
Thermal Resistance Rating				
Maximum Thermal Resistance Junction-Ambient		$R_{\theta JA}$	110	℃ / W
Maximum Thermal Resistance Junction-Case		$R_{\theta JC}$	3.29	℃ / W

Notes:

1. L=30mH,I_{AS}=2.37A, V_{DD}=60V, R_G=25Ω, Starting T_J =25℃

ELECTRICAL CHARACTERISTICS (T_J = 25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	650	-	-	V	V_{GS}=0, I_D= 250μA
Gate-Threshold Voltage	$V_{GS(th)}$	2	-	4	V	V_{DS}=V_{GS}, I_D=250μA
Gate-Source Leakage Current	I_{GSS}	-	-	±100	nA	V_{GS}= ±30V
Drain-Source Leakage Current	I_{DSS}	-	-	1	μA	V_{DS}=650V, V_{GS}=0
Static Drain-Source On-Resistance	$R_{DS(ON)}$	-	4.3	4.8	Ω	V_{GS}=10V, I_D=1A
Total Gate Charge [1.2]	Q_g	-	5.83	-	nC	I_D=2A V_{DS}=520V V_{GS}=10V
Gate-Source Charge [1.2]	Q_{gs}	-	1.73	-		
Gate-Drain Change [1.2]	Q_{gd}	-	2	-		
Turn-on Delay Time [1.2]	$T_{d(on)}$	-	10.67	-	nS	V_{DD}=325V I_D=2A R_G=25 Ω
Rise Time [1.2]	T_r	-	20	-		
Turn-off Delay Time [1.2]	$T_{d(off)}$	-	12.4	-		
Fall Time [1.2]	T_f	-	18	-		
Input Capacitance	C_{iss}	-	261.8	-	pF	V_{GS} =0 V_{DS}=25V f =1.0MHz
Output Capacitance	C_{oss}	-	34.3	-		
Reverse Transfer Capacitance	C_{rss}	-	1.3	-		
Source-Drain Diode						
Diode Forward Voltage	V_{SD}	-	-	1.4	V	I_S=2A, V_{GS}=0
Continuous Source Current	I_S	-	-	2	A	Integral Reverse P-N Junction Diode in the MOSFET
Pulsed Source Current	I_{SM}	-	-	8	A	
Reverse Recovery Time	T_{rr}	-	368.88	-	ns	I_S=2A,V_{GS}=0, dI_F/dt=100A/μS
Reverse Recovery Charge	Q_{rr}	-	1.08	-	μC	

Notes:
1. Pulse Test: Pulse width ≦300μS, Duty cycle≦2%
2. Essentially independent of operating temperature.

CHARACTERISTIC CURVES

Figure 1. On-Region Characteristics

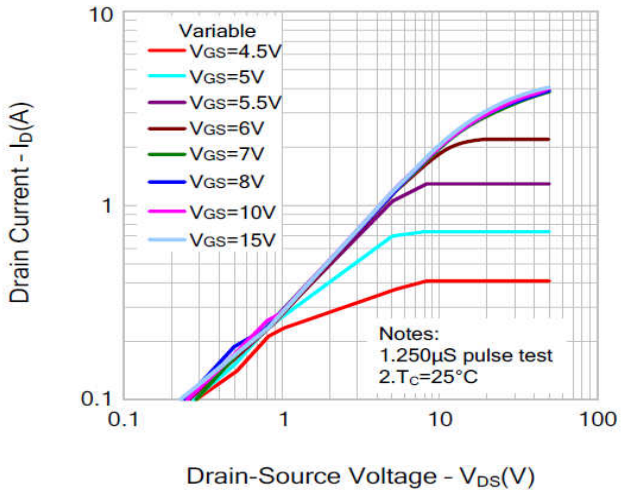


Figure 2. Transfer Characteristics

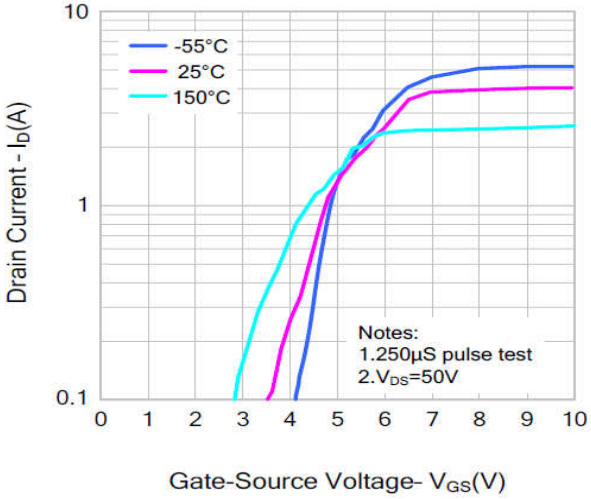


Figure 3. On-Resitance Variation vs. Drain Current and Gate Voltage

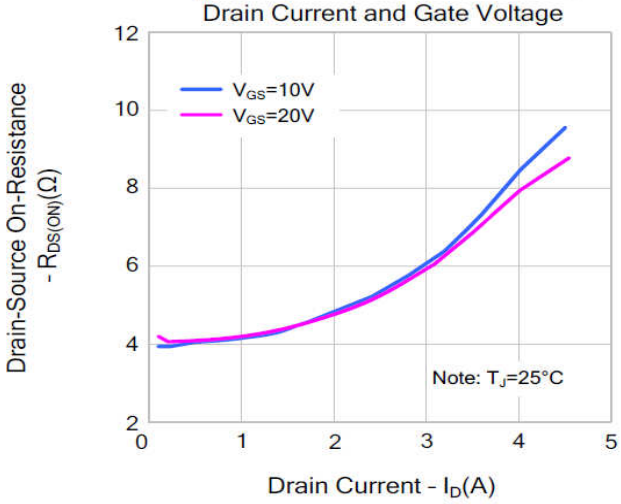


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

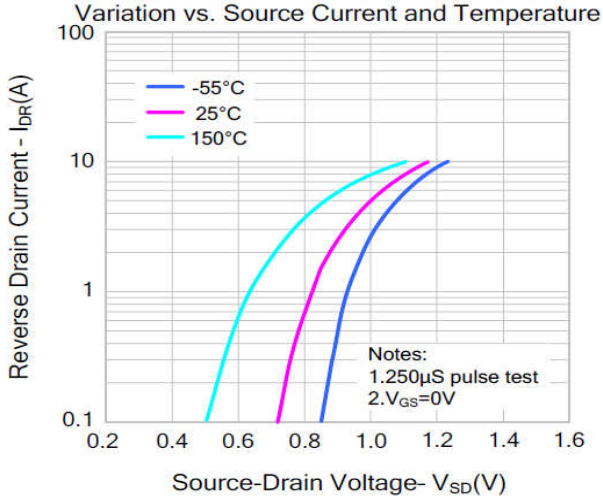


Figure 5. Capacitance Characteristics

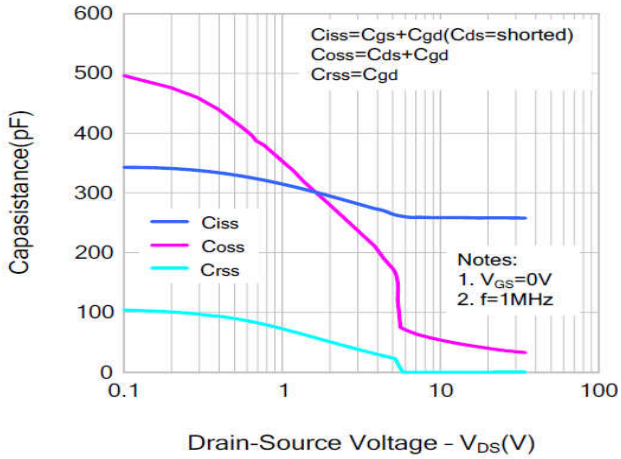
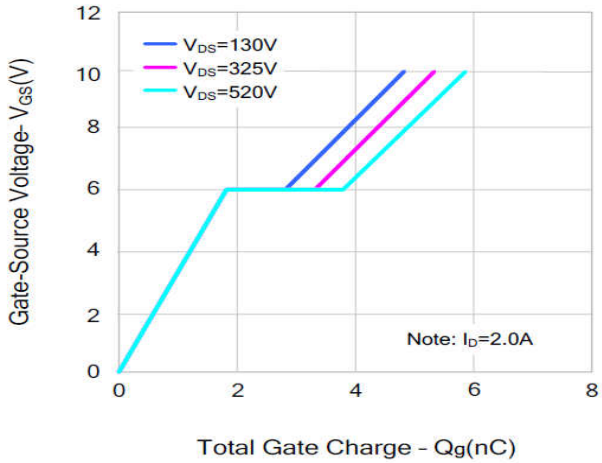


Figure 6. Gate Charge Characteristics



CHARACTERISTIC CURVES

Figure 7. Breakdown Voltage Variation vs. Temperature

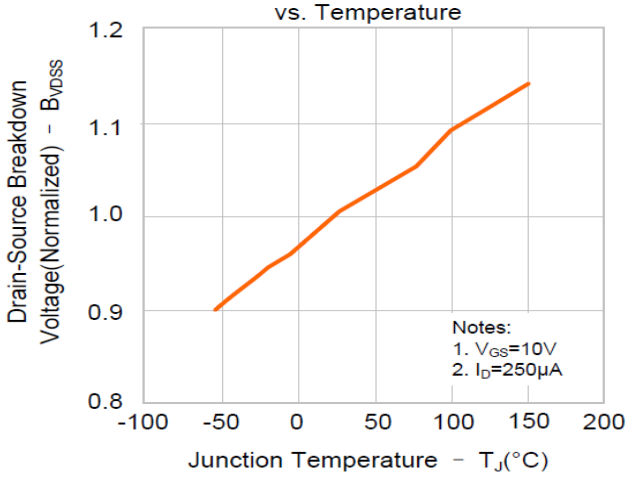


Figure 8. On-resistance Variation vs. Temperature

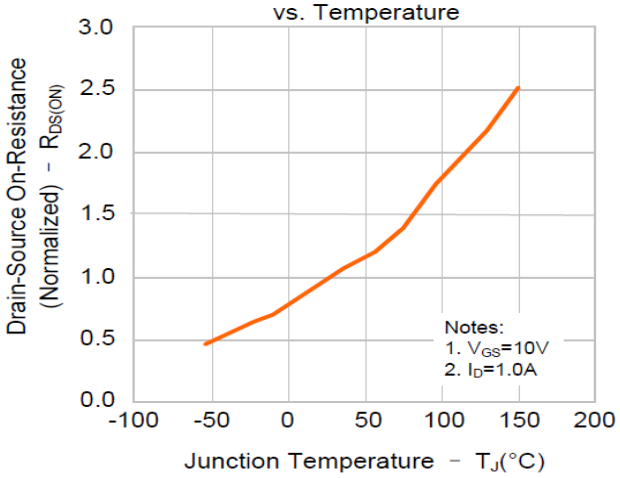


Figure 9 Max. Safe Operating Area

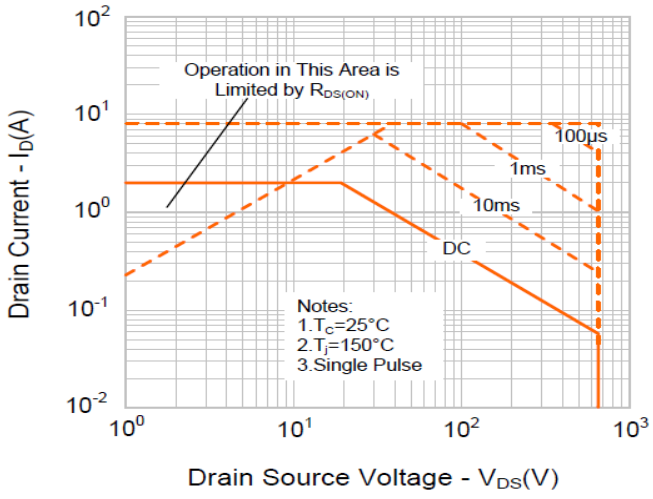
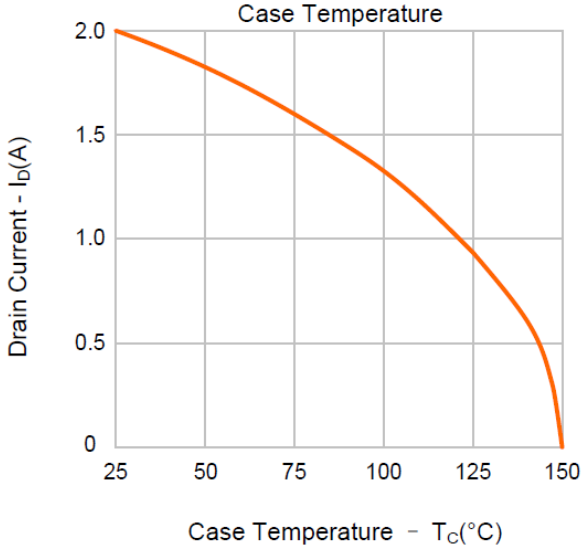
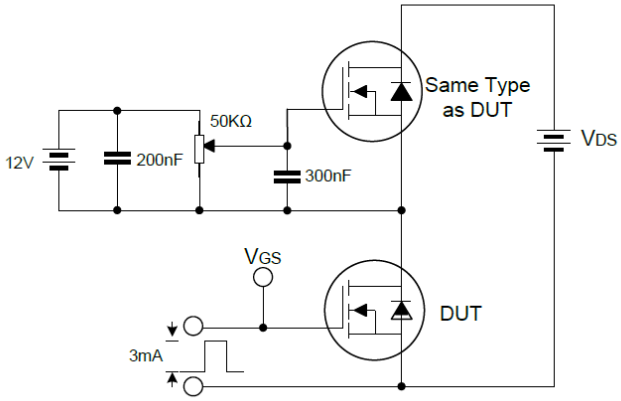


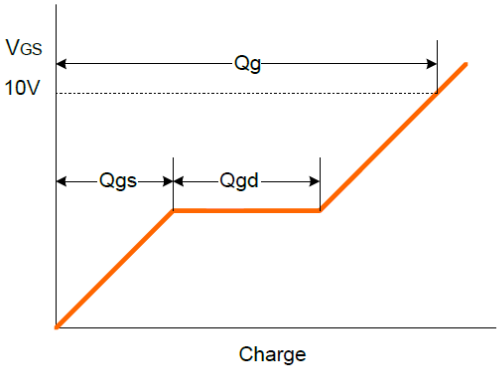
Figure 10. Maximum Drain Current vs. Case Temperature



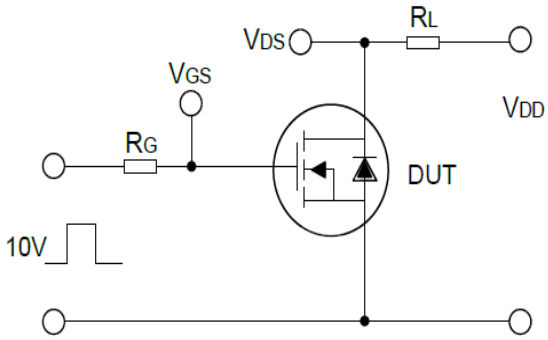
TYPICAL TEST CURVES

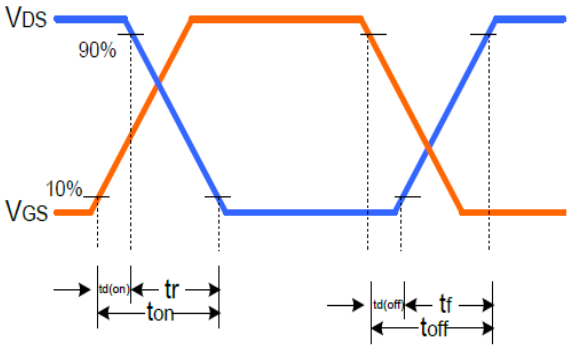
Gate Charge Test Circuit & Waveform





Resistive Switching Test Circuit & Waveform





Unclamped Inductive Switching Test Circuit & Waveform