

RoHS Compliant Product
A suffix of "-C" specifies halogen free

TO-252(D-Pack)

DESCRIPTION

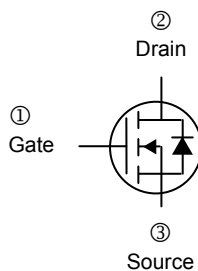
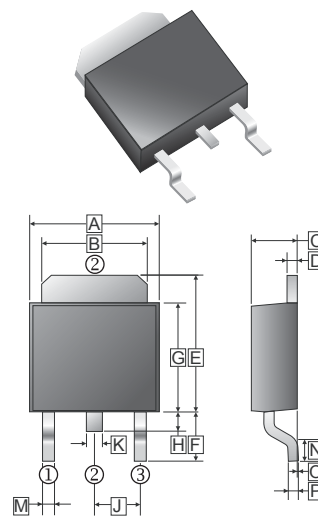
These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology

PRODUCT SUMMARY

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$V_{DS}(V)$	$R_{DS(on)}$ m(Ω)	$I_D(A)$
60	94 @ $V_{GS}=10V$	19
	109 @ $V_{GS}=4.5V$	18



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.4	6.8	J	2.30 REF.	
B	5.20	5.50	K	0.70	0.90
C	2.20	2.40	M	0.50	1.1
D	0.45	0.58	N	0.9	1.6
E	6.8	7.3	O	0	0.15
F	2.40	3.0	P	0.43	0.58
G	5.40	6.2			
H	0.8	1.20			

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^a	$I_D @ T_C=25^\circ C$	19	A
Pulsed Drain Current ^b	I_{DM}	40	A
Continuous Source Current (Diode Conduction) ^a	I_S	30	A
Power Dissipation ^a	$P_D @ T_C=25^\circ C$	50	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ 175	$^\circ C$
THERMAL RESISTANCE RATINGS			
Maximum Thermal Resistance Junction-Ambient ^a	$R_{\theta JA}$	50	$^\circ C / W$
Maximum Thermal Resistance Junction-Case	$R_{\theta JC}$	3.0	$^\circ C / W$

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature.

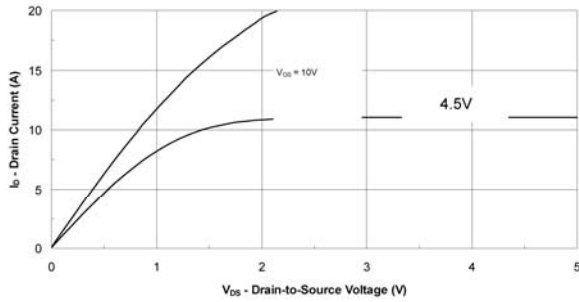
ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	1.0	-	-	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Gate-Body Leakage	I_{GSS}	-	-	± 100	nA	$V_{DS} = 0\text{V}, V_{GS} = 20\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1	μA	$V_{DS} = 48\text{V}, V_{GS} = 0\text{V}$
		-	-	25		$V_{DS} = 48\text{V}, V_{GS} = 0\text{V}, T_J = 55^\circ\text{C}$
On-State Drain Current ^a	$I_{D(ON)}$	34	-	-	A	$V_{DS} = 5\text{V}, V_{GS} = 10\text{V}$
Drain-Source On-Resistance ^a	$R_{DS(ON)}$	-	-	94	m Ω	$V_{GS} = 10\text{V}, I_D = 19\text{A}$
		-	-	109		$V_{GS} = 4.5\text{V}, I_D = 18\text{A}$
Forward Transconductance ^a	g_{fs}	-	22	-	S	$V_{DS} = 15\text{V}, I_D = 19\text{A}$
Diode Forward Voltage	V_{SD}	-	1.1	-	V	$I_S = 24\text{A}, V_{GS} = 0\text{V}$
Dynamic ^b						
Total Gate Charge	Q_g	-	3.6	-	nC	$I_D = 19\text{A}$ $V_{DS} = 15\text{V}$ $V_{GS} = 4.5\text{V}$
Gate-Source Charge	Q_{gs}	-	1.8	-		
Gate-Drain Change	Q_{gd}	-	1.3	-		
Turn-on Delay Time	$T_{d(on)}$	-	16	-	nS	$V_{DD} = 25\text{V}$ $I_D = 24\text{A}$ $R_L = 25\Omega$ $V_{GEN} = 10\text{V}$
Rise Time	T_r	-	5	-		
Turn-off Delay Time	$T_{d(off)}$	-	23	-		
Fall Time	T_f	-	3	-		
Source-Drain Reverse Recovery Time	T_{rr}	-	50	-		$I_F = 24\text{A},$ $Di/Dt = 100\text{A}/\mu\text{s}$

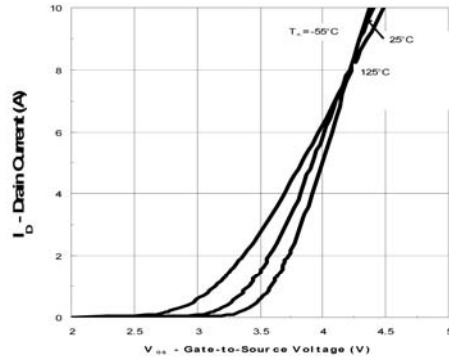
Notes

- a. Pulse test : $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

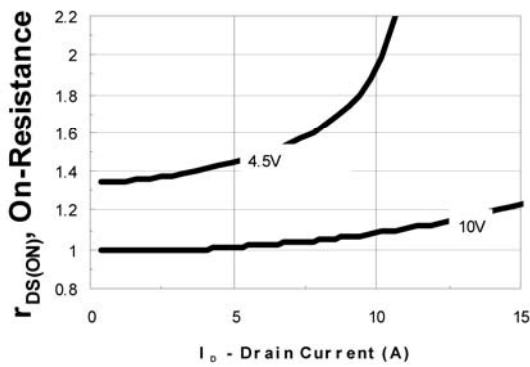
CHARACTERISTICS CURVES



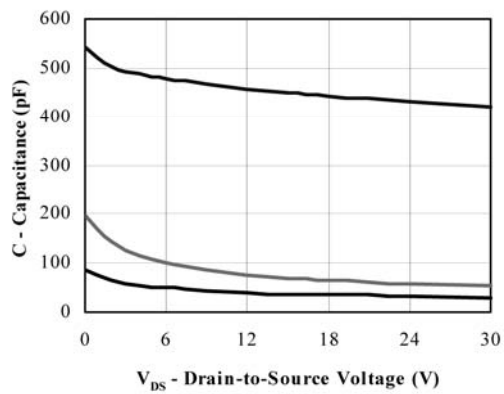
Output Characteristics



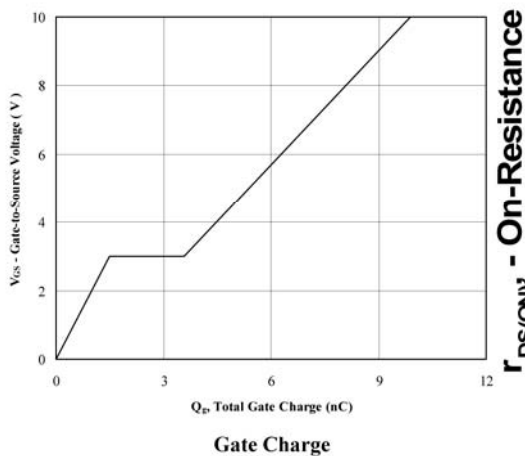
Transfer Characteristics



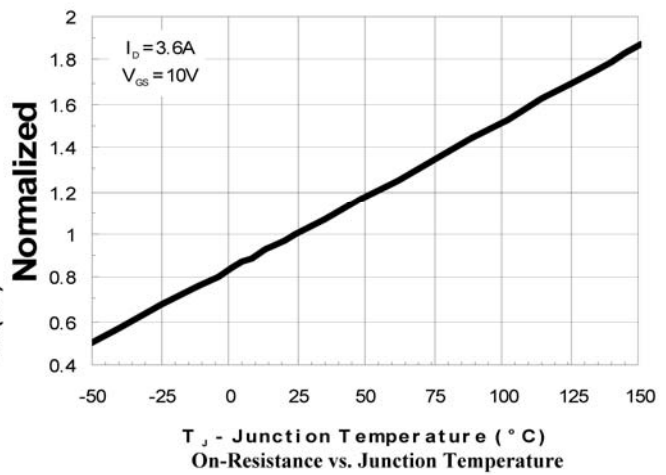
On-Resistance vs. Drain Current



Capacitance

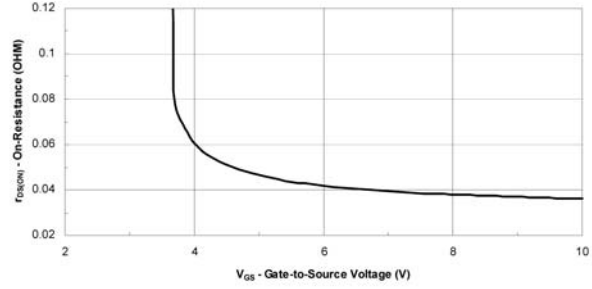
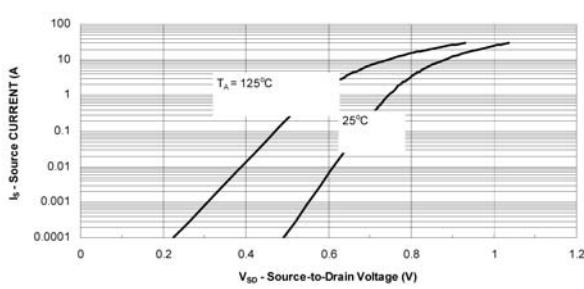


Gate Charge

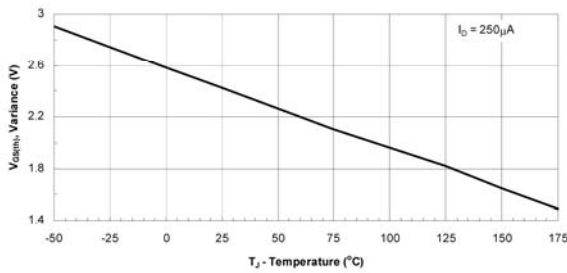


On-Resistance vs. Junction Temperature

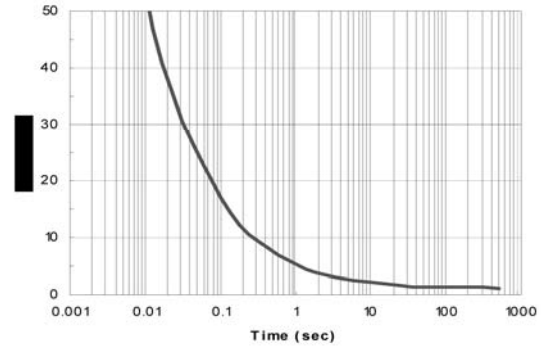
CHARACTERISTICS CURVES



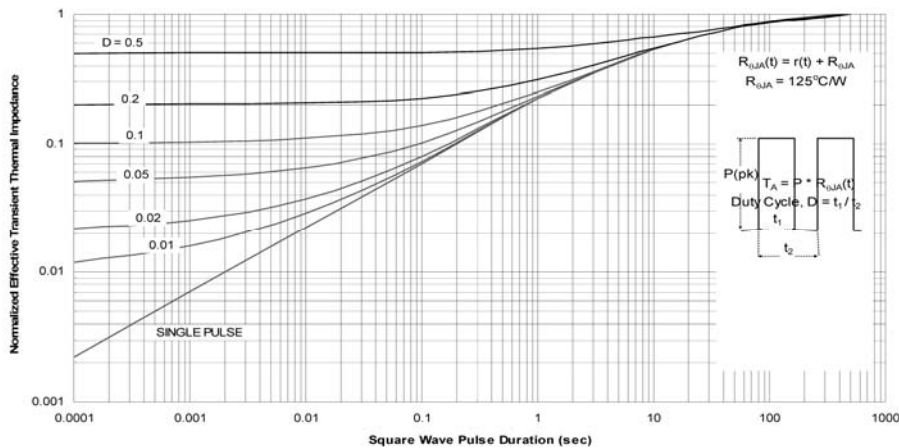
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to Source Voltage



Threshold Voltage



Single Pulse Power

Normalized Thermal Transient Impedance, Junction-to-Ambient