

RoHS Compliant Product  
A suffix of "-C" specifies halogen free

## DESCRIPTION

The SSD25N10-C is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent  $R_{DS(on)}$  and gate charge for most of the synchronous buck converter applications.

The SSD25N10-C meet the RoHS and Green Product requirement with full function reliability approved.

## FEATURES

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Green Device Available

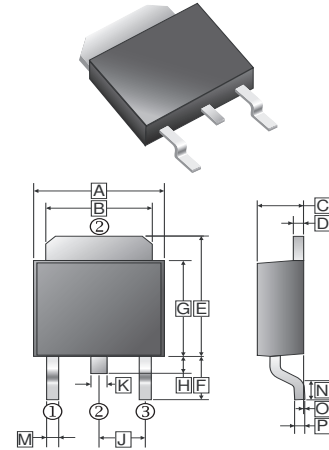
## MARKING



## PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-252	2.5K	13 inch

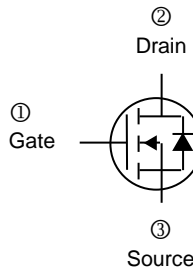
## TO-252(D-Pack)



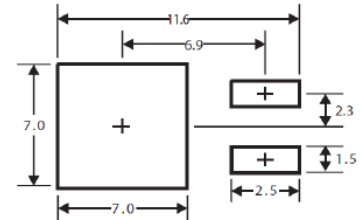
REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.35	6.9	J	2.3 REF.	
B	4.95	5.53	K	0.89 REF.	
C	2.1	2.5	M	0.45	1.14
D	0.41	0.9	N	1.55 Typ.	
E	6	7.5	O	0	0.13
F	2.90 REF.		P	0.58 REF.	
G	5.4	6.4			
H	0.6	1.2			

## ORDER INFORMATION

Part Number	Type
SSD25N10-C	Lead (Pb)-free and Halogen-free



## Mounting Pad Layout



\*Dimensions in millimeters

## ABSOLUTE MAXIMUM RATINGS ( $T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current @ $V_{GS}=10\text{V}$ <sup>1</sup>	$I_D$	$T_C=25^\circ\text{C}$	25
		$T_C=100^\circ\text{C}$	15
Pulsed Drain Current <sup>3</sup>	$I_{DM}$	45	A
Total Power Dissipation	$P_D$	$T_C=25^\circ\text{C}$	52
		$T_A=25^\circ\text{C}$	2
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~150	$^\circ\text{C}$
<b>Thermal Resistance Rating</b>			
Maximum Thermal Resistance Junction-Ambient <sup>1</sup>	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Maximum Thermal Resistance Junction-Ambient <sup>2</sup>		110	
Maximum Thermal Resistance Junction-Case <sup>1</sup>	$R_{\theta JC}$	2.4	

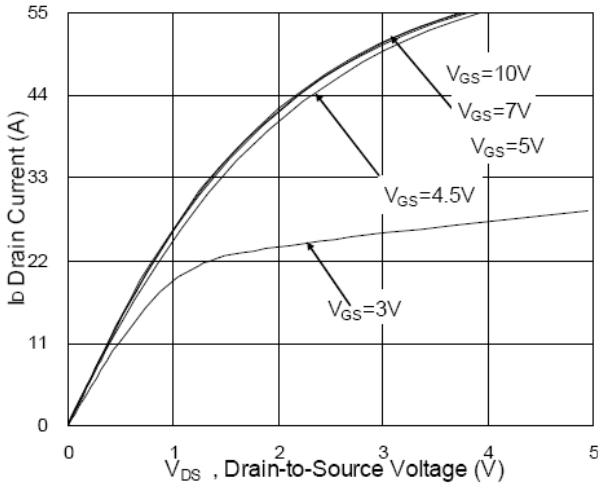
**ELECTRICAL CHARACTERISTICS** ( $T_J=25^\circ C$  unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Teat Conditions	
Drain-Source Breakdown Voltage	$BV_{DSS}$	100	-	-	V	$V_{GS}=0, I_D=250\mu A$	
Gate-Threshold Voltage	$V_{GS(th)}$	1	-	2.5	V	$V_{DS}=V_{GS}, I_D=250\mu A$	
Gate-Source Leakage Current	$I_{GSS}$	-	-	$\pm 100$	nA	$V_{GS}=\pm 20V$	
Drain-Source Leakage Current	$I_{DSS}$	$T_J=25^\circ C$	-	-	1	$\mu A$	$V_{DS}=80V, V_{GS}=0$
		$T_J=55^\circ C$	-	-	100		$V_{DS}=80V, V_{GS}=0$
Static Drain-Source On-Resistance <sup>4</sup>	$R_{DS(ON)}$	-	43	48	m $\Omega$	$V_{GS}=10V, I_D=25A$	
		-	45	50		$V_{GS}=4.5V, I_D=15A$	
Total Gate Charge	$Q_g$	-	59	-	nC	$I_D=20A$ $V_{DS}=80V$ $V_{GS}=10V$	
Gate-Source Charge	$Q_{gs}$	-	9.7	-			
Gate-Drain Change	$Q_{gd}$	-	11.8	-			
Turn-on Delay Time <sup>2</sup>	$T_{d(on)}$	-	10.4	-	nS	$V_{DD}=50V$ $I_D=20A$ $V_{GS}=10V$ $R_G=3.3\Omega$	
Rise Time	$T_r$	-	46	-			
Turn-off Delay Time	$T_{d(off)}$	-	54	-			
Fall Time	$T_f$	-	10	-			
Input Capacitance	$C_{iss}$	-	3848	-	pF	$V_{GS}=0$ $V_{DS}=15V$ $f=1MHz$	
Output Capacitance	$C_{oss}$	-	137	-			
Reverse Transfer Capacitance	$C_{rss}$	-	82	-			
Gate Resistance	$R_g$	-	1.6	4	$\Omega$	$f=1MHz$	
<b>Source-Drain Diode</b>							
Continuous Source Current <sup>1</sup>	$I_S$	-	-	25	A	$V_D=V_G=0, \text{ Force Current}$	
Pulsed Source Current <sup>3</sup>	$I_{SM}$	-	-	45	A		
Diode Forward Voltage <sup>4</sup>	$V_{SD}$	-	-	1.2	V	$I_S=1A, V_{GS}=0, T_J=25^\circ C$	
Reverse Recovery Time	$T_{rr}$	-	30	-	nS	$I_F=20A, di/dt=100A/\mu s,$ $T_J=25^\circ C$	
Reverse Recovery Charge	$Q_{rr}$	-	37	-	nC		

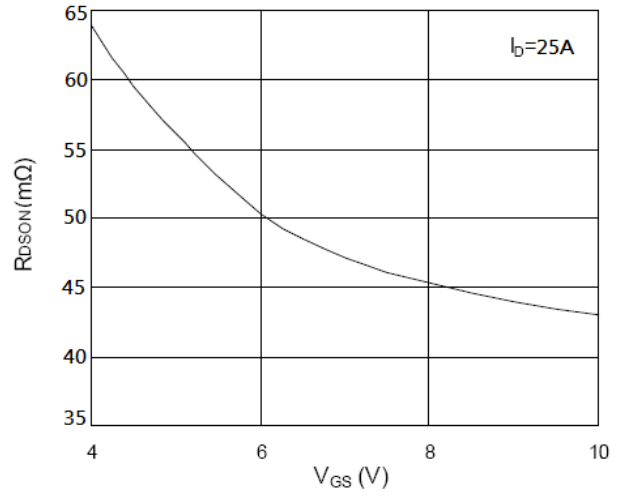
Notes:

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2oz copper.
2. When mounted on minimum pad of 2oz copper.
3. The power dissipation is limited by 150°C junction temperature.
4. The data tested by pulsed, pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .

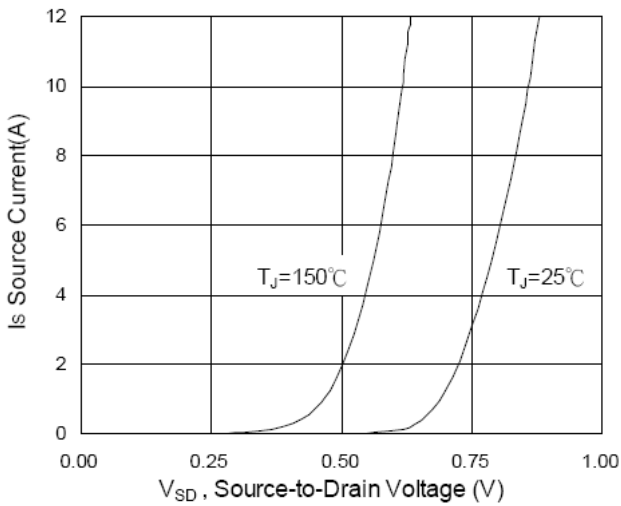
**CHARACTERISTIC CURVES**



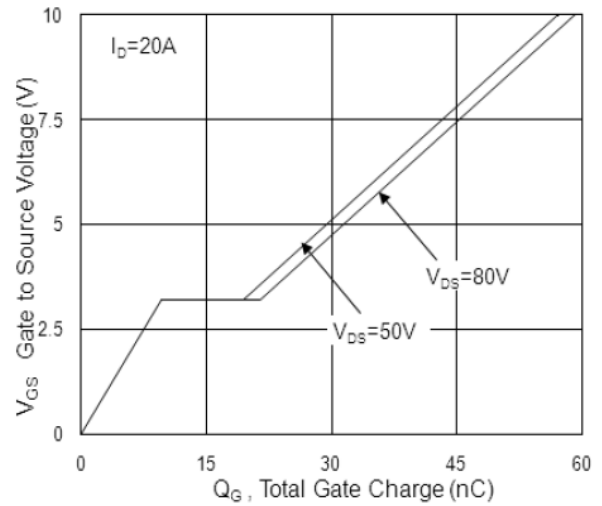
**Fig.1 Typical Output Characteristics**



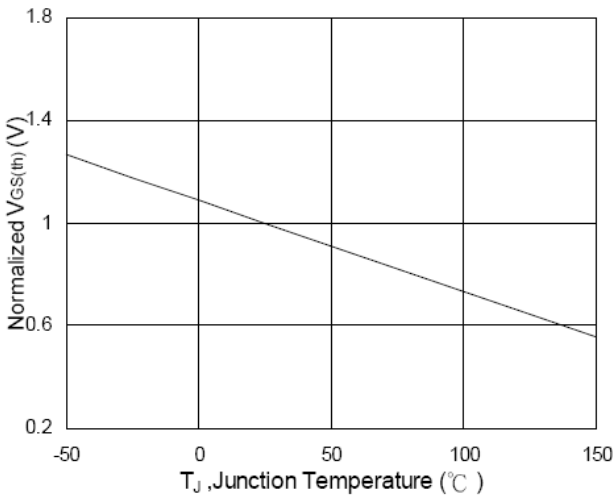
**Fig.2 On-Resistance vs. Gate-Source**



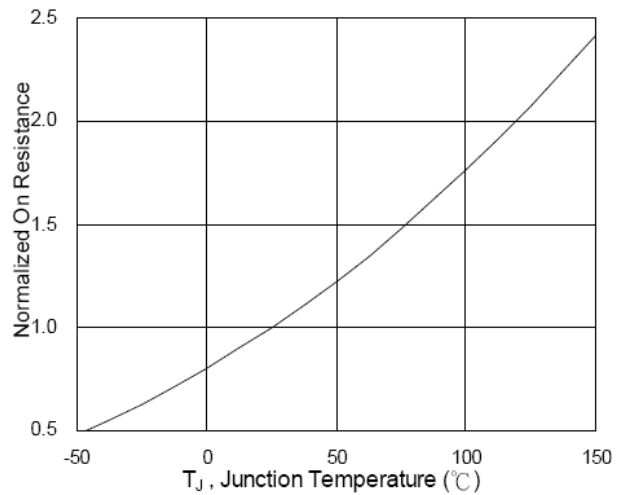
**Fig.3 Forward Characteristics Of Reverse**



**Fig.4 Gate-Charge Characteristics**

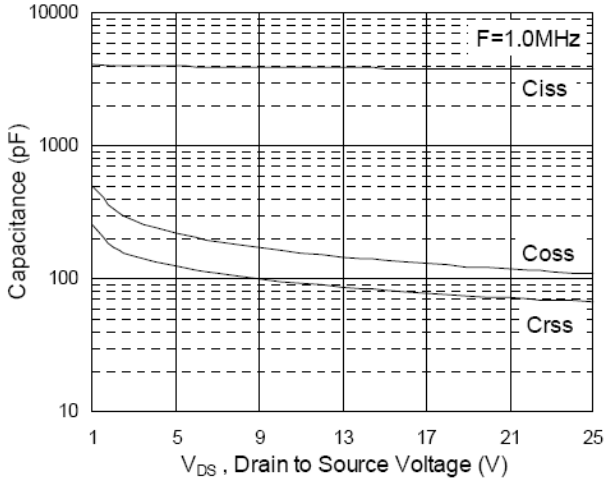


**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**

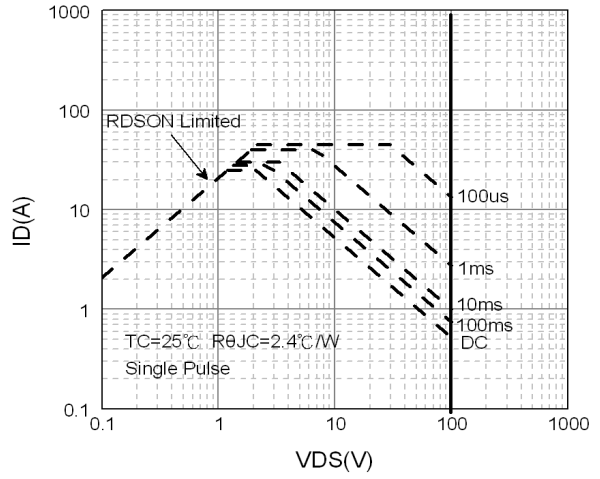


**Fig.6 Normalized  $R_{DS(ON)}$  vs.  $T_J$**

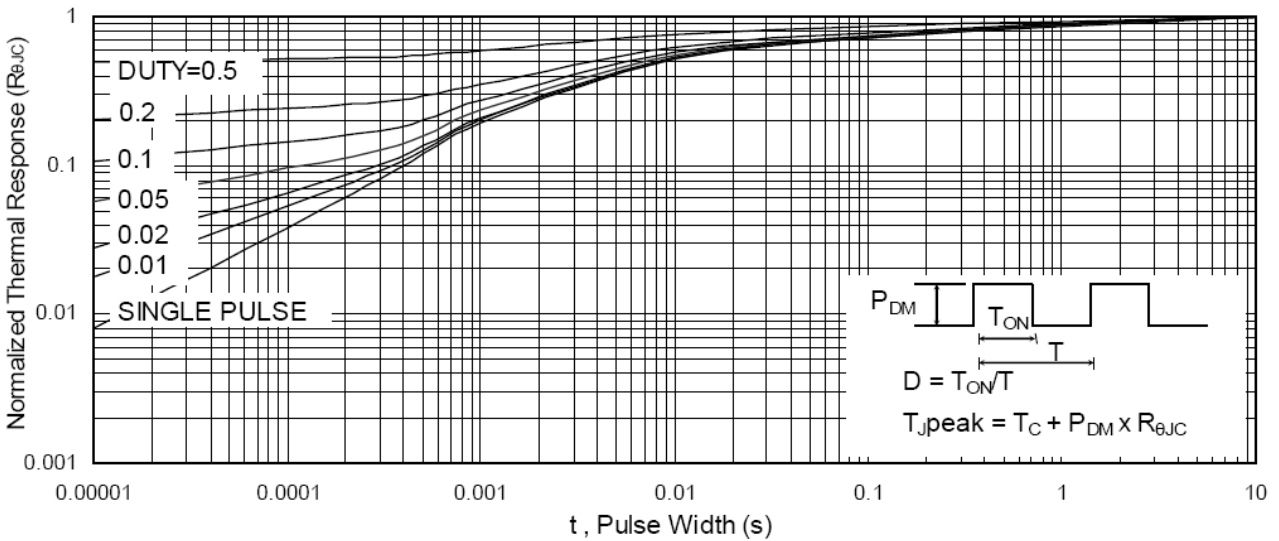
**CHARACTERISTIC CURVES**



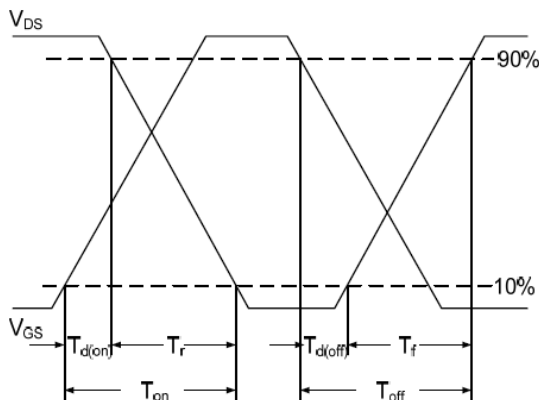
**Fig.7 Capacitance**



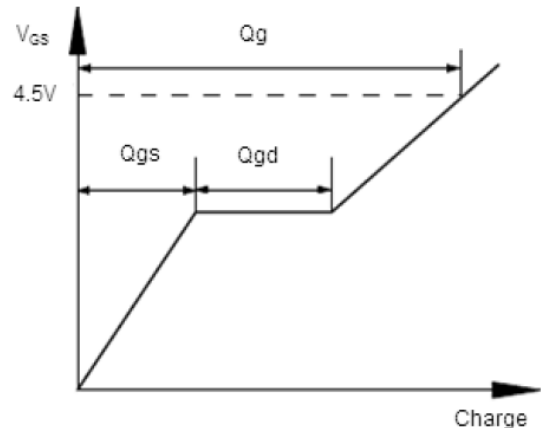
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching Time Waveform**



**Fig.11 Gate Charge Waveform**