

RoHS Compliant Product  
A suffix of "-C" specifies halogen free

## DESCRIPTION

The SSD35P03 is the highest performance trench P-ch MOSFETs with extreme high cell density, which provide excellent  $R_{DS(ON)}$  and gate charge for most of the synchronous buck converter applications.

The SSD35P03 meet the RoHS and Green Product with Function reliability approved.

## FEATURES

- Advanced high Cell Density Trench Technology
- Super Low Gate Charge
- Green Device Available
- TO-252 Package

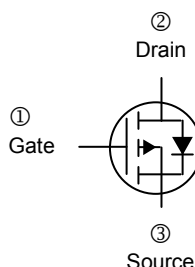
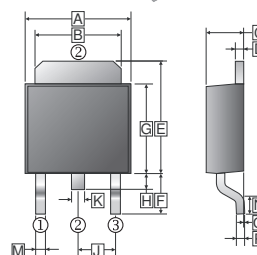
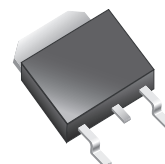
## MARKING



## PACKAGE INFORMATION

Package	MPQ	Leader Size
TO-252	2.5K	13 inch

### TO-252(D-Pack)



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.35	6.90	J	2.336 REF.	
B	4.95	5.53	K	0.89 REF.	
C	2.10	2.50	M	0.45	1.14
D	0.665 Typ.		N	1.55 Typ.	
E	6.0	7.5	O	0	0.13
F	2.90 REF.		P	0.58 REF.	
G	5.40	6.40			
H	0.60	1.20			

## ABSOLUTE MAXIMUM RATINGS ( $T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit	
Drain-Source Voltage	$V_{DS}$	-30	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current, @ $V_{GS}=10\text{V}$ <sup>1</sup>	$I_D$	$T_C=25^\circ\text{C}$	-35	A
		$T_C=100^\circ\text{C}$	-22	A
Pulsed Drain Current <sup>2</sup>	$I_{DM}$	-80	A	
Power Dissipation	$P_D$	50	W	
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 ~ 150	$^\circ\text{C}$	
<b>Thermal Resistance Ratings</b>				
Maximum Thermal Resistance Junction-Ambient <sup>1</sup>	$R_{\theta JA}$	62.5	$^\circ\text{C} / \text{W}$	
Maximum Thermal Resistance Junction-Case <sup>1</sup>	$R_{\theta JC}$	2.5		

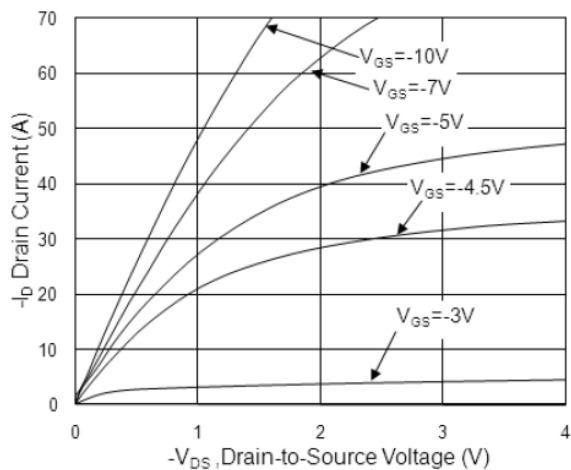
**ELECTRICAL CHARACTERISTICS** ( $T_J=25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	
Drain-Source Breakdown Voltage	$BV_{DSS}$	-30	-	-	V	$V_{GS}=0, I_D = -250\mu\text{A}$	
Gate Threshold Voltage	$V_{GS(th)}$	-1	-	-2.5	V	$V_{DS}=V_{GS}, I_D = -250\mu\text{A}$	
Forward Transfer conductance	$g_{fs}$	-	20	-	S	$V_{DS} = -5\text{V}, I_D = -18\text{A}$	
Gate-Source Leakage Current	$I_{GSS}$	-	-	$\pm 100$	nA	$V_{GS} = \pm 20\text{V}$	
Drain-Source Leakage Current	$I_{DSS}$	$T_J=25^\circ\text{C}$	-	-	-1	$\mu\text{A}$	$V_{DS} = -24\text{V}, V_{GS}=0$
		$T_J=55^\circ\text{C}$	-	-	-5		
Static Drain-Source On-Resistance <sup>3</sup>	$R_{DS(ON)}$	-	-	28	m $\Omega$	$V_{GS} = -10\text{V}, I_D = -18\text{A}$	
		-	-	40		$V_{GS} = -4.5\text{V}, I_D = -10\text{A}$	
Total Gate Charge	$Q_g$	-	18	-	nC	$I_D = -18\text{A}$ $V_{DS} = -15\text{V}$ $V_{GS} = -10\text{V}$	
Gate-Source Charge	$Q_{gs}$	-	3.3	-			
Gate-Drain Charge	$Q_{gd}$	-	4.9	-			
Turn-on Delay Time	$T_{d(on)}$	-	7	-	nS	$V_{DD} = -15\text{V}$ $I_D = -18\text{A}$ $V_{GS} = -10\text{V}$ $R_G = 3\Omega$	
Rise Time	$T_r$	-	11	-			
Turn-off Delay Time	$T_{d(off)}$	-	27	-			
Fall Time	$T_f$	-	8	-			
Input Capacitance	$C_{iss}$	-	1345	-	pF	$V_{GS}=0$ $V_{DS} = -15\text{V}$ $f=1.0\text{MHz}$	
Output Capacitance	$C_{oss}$	-	194	-			
Reverse Transfer Capacitance	$C_{rss}$	-	158	-			
<b>Source-Drain Diode</b>							
Forward On Voltage <sup>3</sup>	$V_{SD}$	-	-	-1.2	V	$I_S = -1\text{A}, V_{GS}=0$	
Reverse Recovery Time	$T_{rr}$	-	24	-	nS	$I_F = -18\text{A}, di/dt=100\text{A}/\mu\text{s}$	
Reverse Recovery Charge	$Q_{rr}$	-	14	-	nC	$T_J=25^\circ\text{C}$	

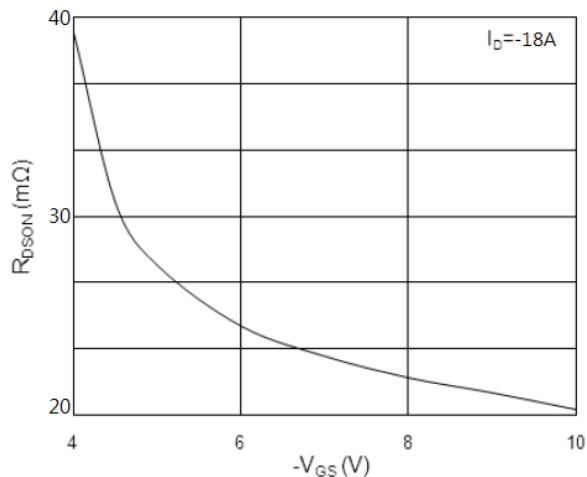
Notes:

1. The date tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2oz copper.
2. The power dissipation is limited by 150°C junction temperature.
3. The data tested by pulsed, pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$ .

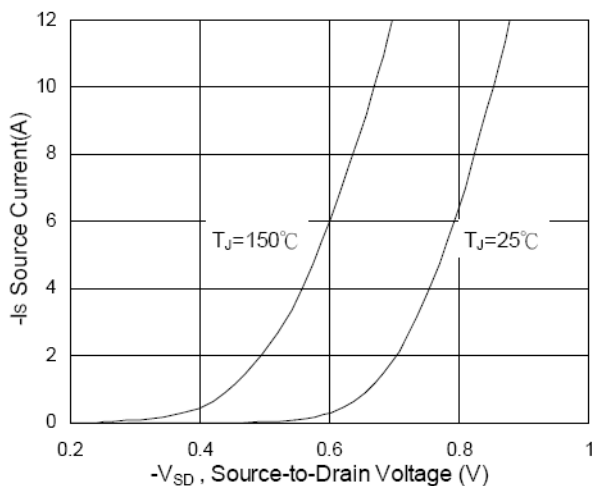
**TYPICAL CHARACTERISTICS CURVE**



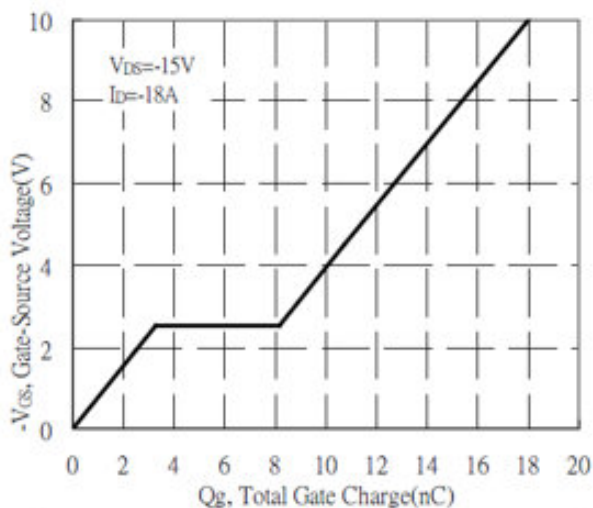
**Fig.1 Typical Output Characteristics**



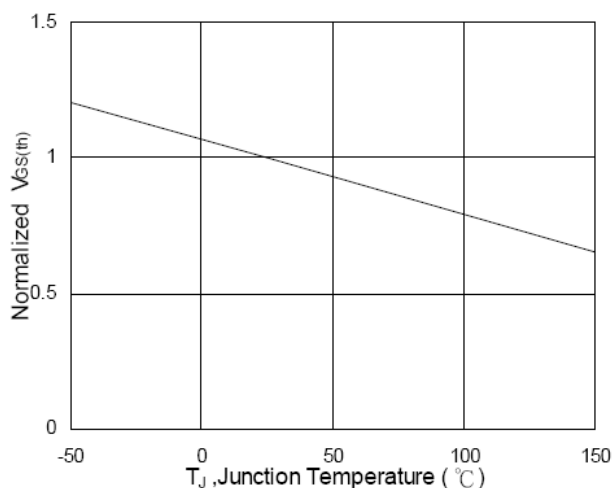
**Fig.2 On-Resistance v.s Gate-Source**



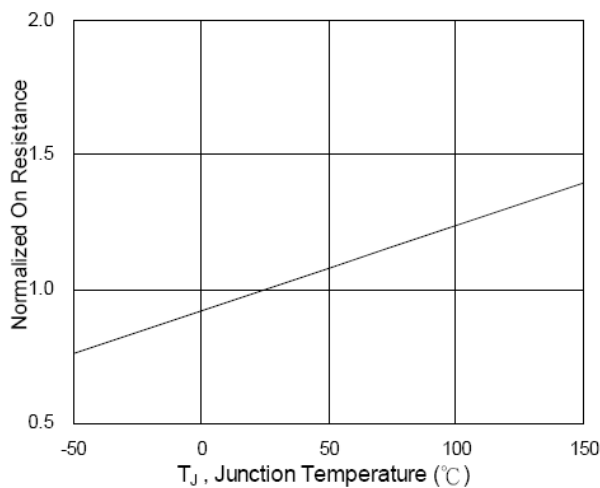
**Fig.3 Forward Characteristics of Reverse**



**Fig.4 Gate-Charge Characteristics**



**Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_J$**



**Fig.6 Normalized  $R_{DS(on)}$  v.s  $T_J$**

**TYPICAL CHARACTERISTICS CURVE**

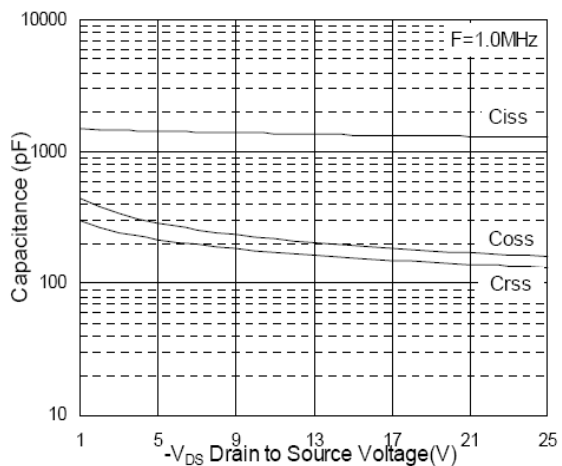


Fig.7 Capacitance

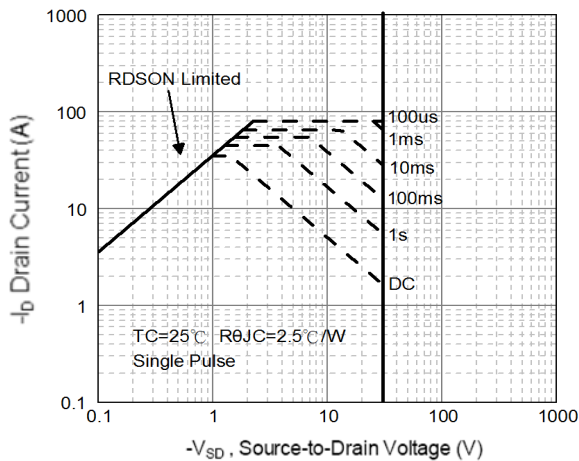


Fig.8 Safe Operating Area

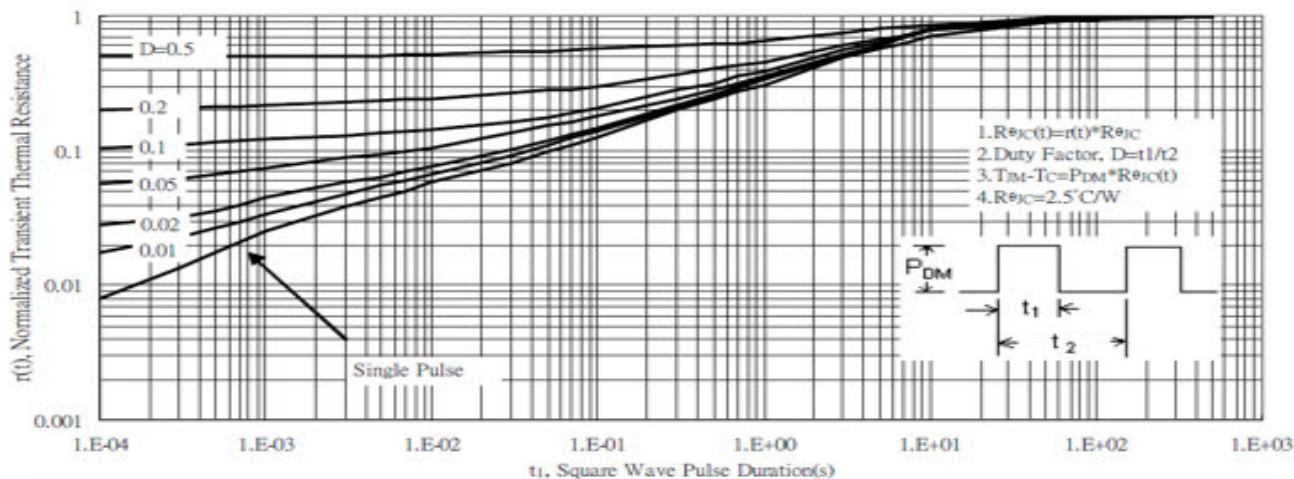


Fig.9 Normalized Maximum Transient Thermal Impedance

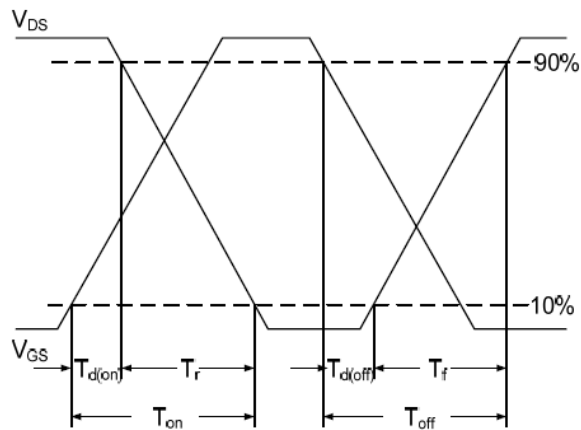


Fig.10 Switching Time Waveform

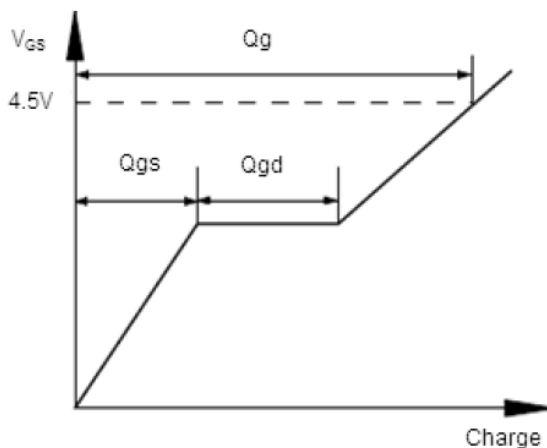


Fig.11 Gate Charge Waveform