Elektronische Bauelemente

SSD60N04-12D

N-Ch Enhancement Mode Power MOSFET

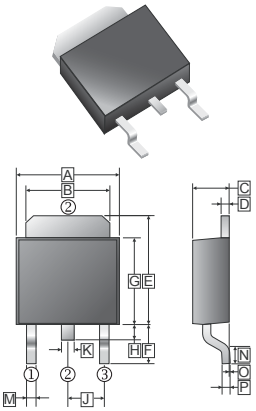
53A, 40V, $R_{DS(ON)}$ 12mΩ

RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable And battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

TO-252(D-Pack)



FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Low thermal impedance copper leadframe DPAK saves board space.
- Fast switching speed.
- High performance trench technology.

PRODUCT SUMMARY

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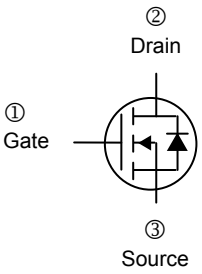
V_{DS}(V)	R_{DS}(on) m(Ω)	I_D(A)
40	12@V_{GS}= 10V	53
	14@V_{GS}= 4.5V	49



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	6.4	6.8	J	2.30 REF.	
B	5.20	5.50	K	0.70	0.90
C	2.20	2.40	M	0.50	1.1
D	0.45	0.58	N	0.9	1.6
E	6.8	7.3	O	0	0.15
F	2.40	3.0	P	0.43	0.58
G	5.40	6.2			
H	0.8	1.20			

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current [a]	I_D @T_A=25℃	53	A
Pulsed Drain Current [b]	I_{DM}	40	A
Continuous Source Current (Diode Conduction) [a]	I_S	30	A
Total Power Dissipation [a]	P_D @T_A=25℃	50	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ 175	°C
THERMAL RESISTANCE RATINGS			
Maximum Thermal Resistance Junction-Ambient [a]	$R_{\theta JA}$	50	°C / W
Maximum Thermal Resistance Junction-Case	$R_{\theta JC}$	3.0	°C / W

Notes :
a. Surface Mounted on 1" x 1" FR4 Board.
b. Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

PARAMETER	SYMBO	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	1.0	-	-	V	V_{DS}= V_{GS}, I_D = 250 μA
Gate-Body Leakage	I_{GSS}	-	-	±100	nA	V_{DS} = 0V, V_{GS}= 20V
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1	μA	V_{DS}= 32V, V_{GS}= 0V
		-	-	25		V_{DS}= 32V, V_{GS}= 0V, T_J=55°C
On-State Drain Current [a]	$I_{D(on)}$	34	-	-	A	V_{DS} = 5V, V_{GS}= 10V
Drain-Source On-Resistance [a]	$R_{DS(ON)}$	-	-	12	mΩ	V_{GS}= 10V, I_D= 53 A
		-	-	14		V_{GS}= 4.5V, I_D= 49 A
Forward Transconductance [a]	g_{fs}	-	22	-	S	V_{DS}= 15V, I_D= 53 A
Diode Forward Voltage	V_{SD}	-	1.1	-	V	I_S= 34 A, V_{GS}= 0 V
Dynamic [b]						
Total Gate Charge	Q_g	-	4.0	-	nC	V_{DS} = 15 V V_{GS} = 4.5 V I_D = 53 A
Gate-Source Charge	Q_{gs}	-	1.1	-		
Gate-Drain Charge	Q_{gd}	-	1.4	-		
Turn-on Delay Time	$T_{d(on)}$	-	16	-	nS	V_{DD}= 25 V I_D= 34 A V_{GEN} = 10 V R_L= 25 Ω
Rise Time	T_r	-	5	-		
Turn-off Delay Time	$T_{d(off)}$	-	23	-		
Fall Time	T_f	-	3	-		

Notes
a. Pulse test：Pulse width ≦ 300 μs, duty cycle ≦ 2%.
b. Guaranteed by design, not subject to production testing.