Elektronische Bauelemente

SSU75N20-C

75A, 200V, $R_{DS(ON)}$ 18.5mΩ
N-Channel Enhancement Mode Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen and lead-free

DESCRIPTION

The SSU75N20-C is the highest performance N-Ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The SSU75N20-C meet the RoHS and Green Product requirement with full function reliability approved.

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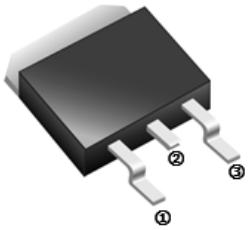
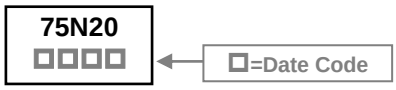
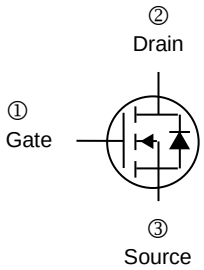


FEATURES

- Advanced Trench MOS Technology
- 100% EAS Guaranteed
- High Speed Power Smooth Switching
- Enhanced Avalanche Ruggedness
- Green Device Available

MARKING





ORDER INFORMATION

Part Number	Type
SSU75N20-C	Lead (Pb)-free and Halogen-free

ABSOLUTE MAXIMUM RATINGS (T_J=25°C unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	200	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current @Silicon Limited	T_C=25°C	I_D	75	A
	T_C=100°C		53	
Pulsed Drain Current		I_{DM}	280	A
Power Dissipation	T_C=25°C	P_D	300	W
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55~175	°C
Thermal Resistance Ratings				
Thermal Resistance Junction-Ambient		$R_{\theta JA}$	60	°C/W
Thermal Resistance Junction-Case		$R_{\theta JC}$	0.5	

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test conditions
Drain-Source Breakdown Voltage		BV_{DSS}	200	-	-	V	V_{GS}=0V, I_D=250μA
Gate Threshold Voltage		$V_{GS(th)}$	2	-	4	V	V_{DS}=V_{GS}, I_D=250μA
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}=±20V, V_{DS}=0V
Drain-Source Leakage Current	T_J=25°C	I_{DSS}	-	-	1	μA	V_{DS}=200V, V_{GS}=0V
	T_J=100°C		-	-	100		
Static Drain-Source On-Resistance		$R_{DS(ON)}$	-	15.5	18.5	mΩ	V_{GS}=10V, I_D=10A
Gate Resistance		R_g	-	1.8	-	Ω	V_{GS}=V_{DS}=0V, f=1MHz
Forward Transconductance		g_{fs}	-	70	-	S	V_{DS}=5V, I_D=20A
Total Gate Charge		Q_g	-	102	-	nC	V_{DS}=100V V_{GS}=10V I_D=20A
Gate-Source Charge		Q_{gs}	-	24	-		
Gate-Drain (“Miller”) Change		Q_{gd}	-	38	-		
Turn-on Delay Time		$T_{d(on)}$	-	21	-	nS	V_{DD}=100V V_{GS}=10V I_D=20A R_G=10Ω
Rise Time		T_r	-	16	-		
Turn-off Delay Time		$T_{d(off)}$	-	38	-		
Fall Time		T_f	-	17	-		
Input Capacitance		C_{iss}	-	5700	-	pF	V_{DS}=100V V_{GS}=0V f=1MHz
Output Capacitance		C_{oss}	-	213	-		
Reverse Transfer Capacitance		C_{rss}	-	60	-		
Source-Drain Diode							
Diode Forward Voltage		V_{SD}	-	-	0.9	V	I_F=20A, V_{GS}=0V
Reverse Recovery Time		T_{rr}	-	112	-	nS	V_R=100V, I_F=20A di/dt=100A/μs
Reverse Recovery Charge		Q_{rr}	-	348	-	nC	

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TYPICAL CHARACTERISTICS CURVE

Fig 1. Typical Output Characteristics

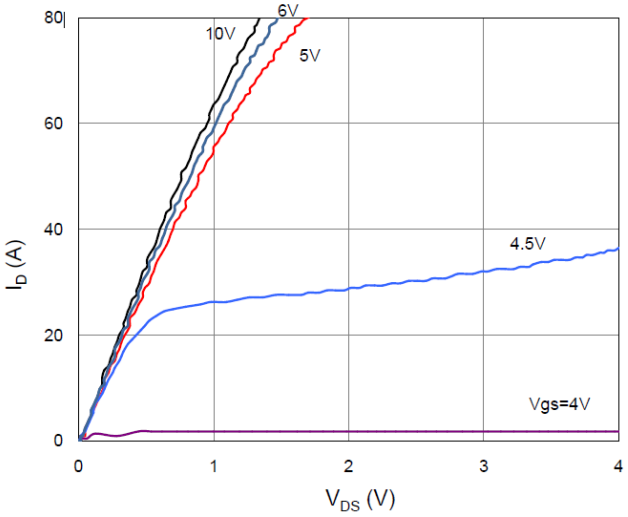


Fig 2. On-Resistance vs. Gate-Source Voltage

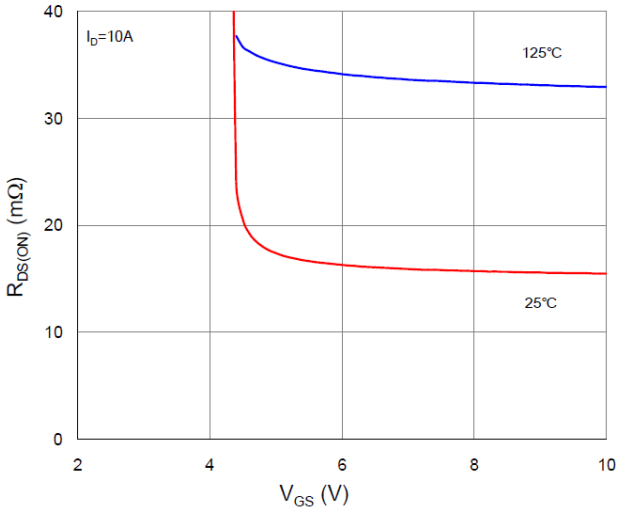


Fig 3. On-Resistance vs. Drain Current and Gate Voltage

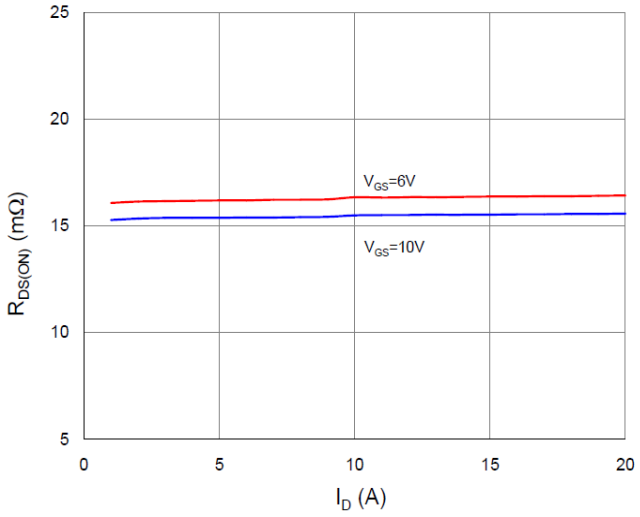


Fig 4. Normalized On-Resistance vs. Junction Temperature

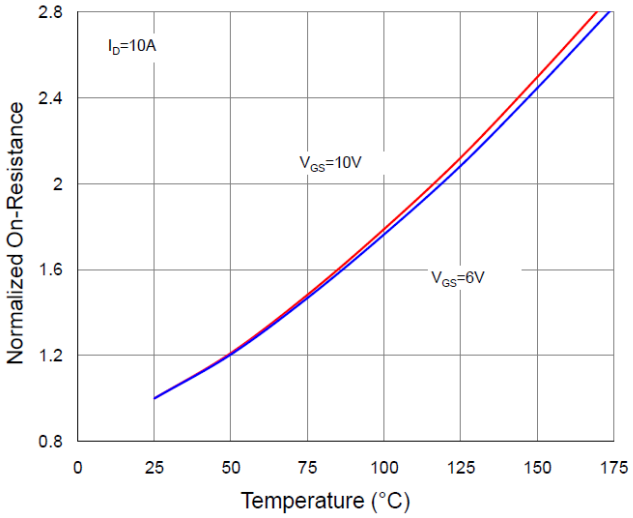


Fig 5. Typical Transfer Characteristics

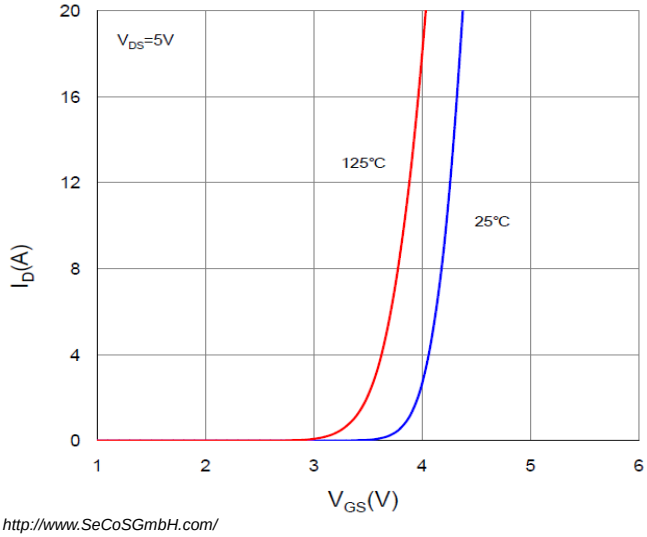
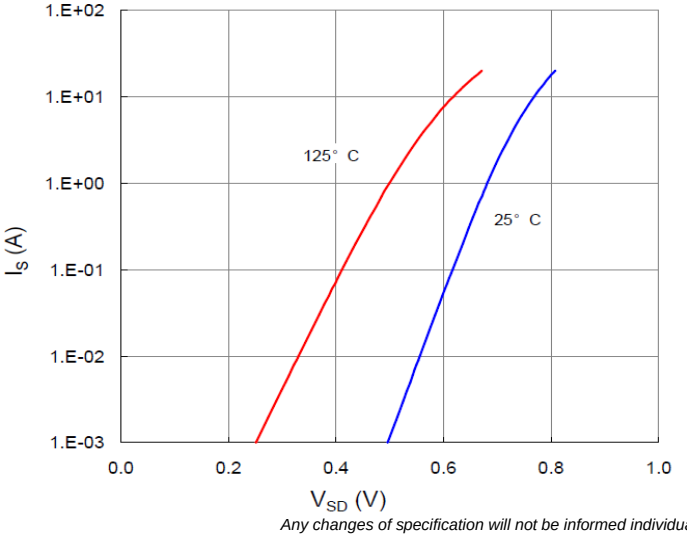


Fig 6. Typical Source-Drain Diode Forward Voltage



TYPICAL CHARACTERISTICS CURVE

Fig 7. Typical Gate-Charge vs. Gate-to-Source Voltage

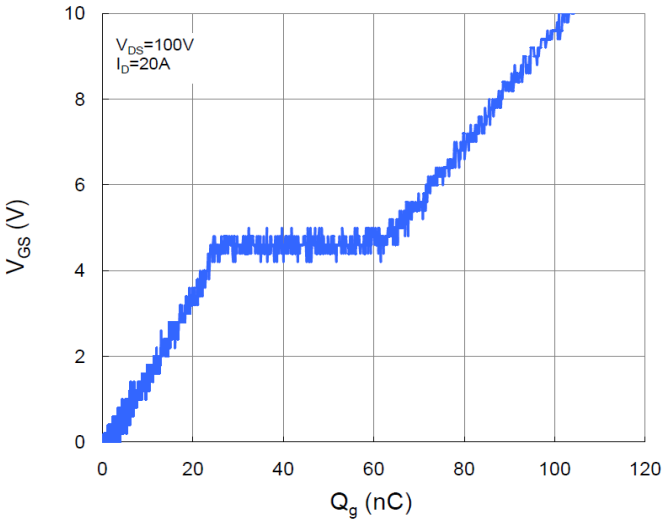


Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

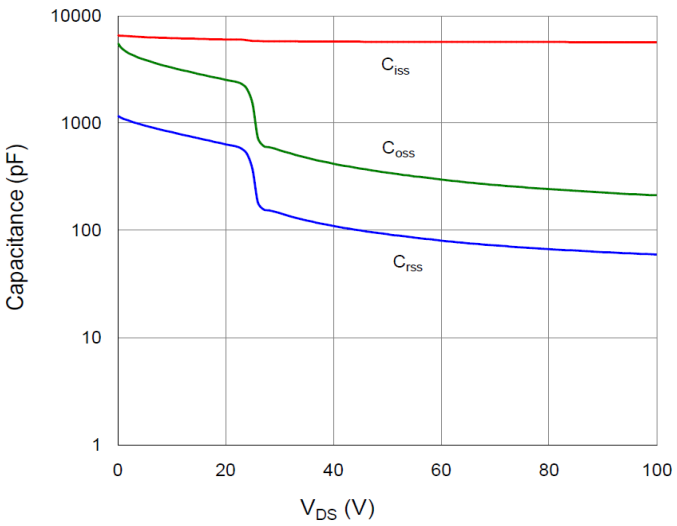


Fig 9. Maximum Safe Operating Area

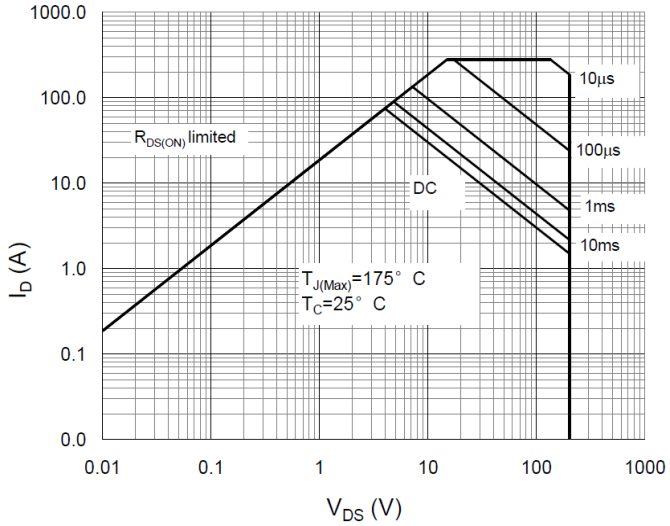


Fig 10. Maximum Drain Current vs. Case Temperature

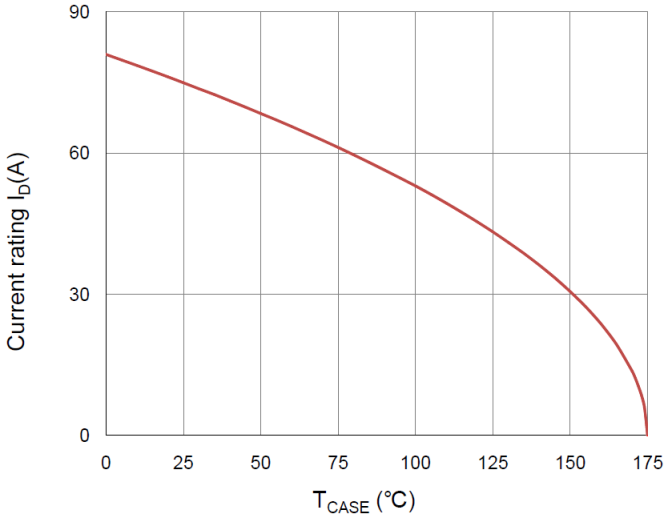
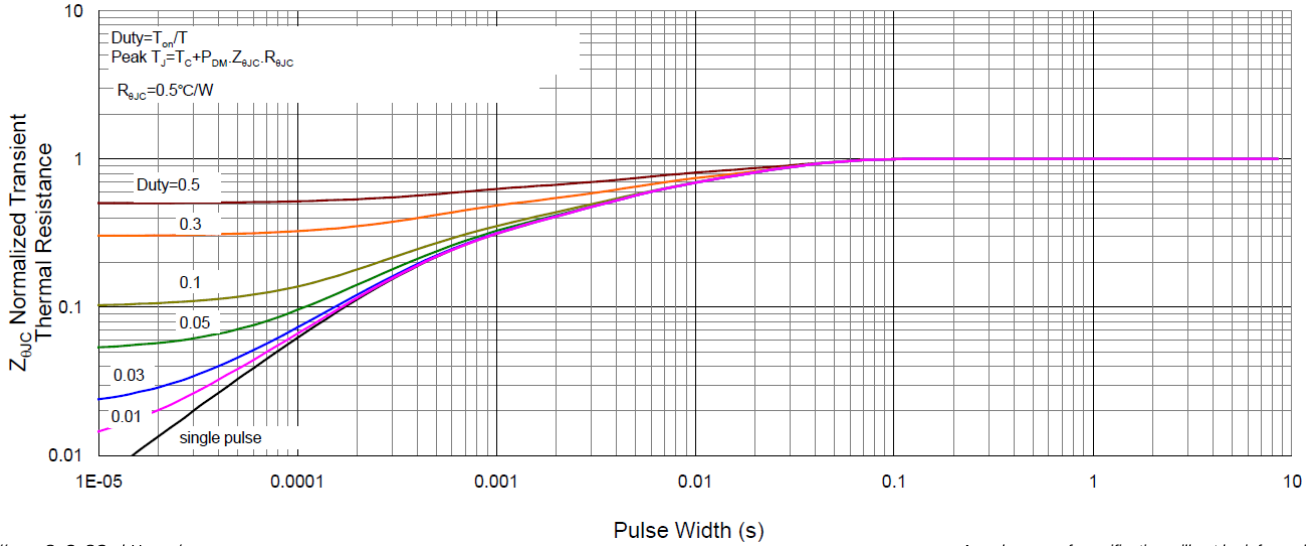


Fig 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



PACKAGE OUTLINE DIMENSIONS

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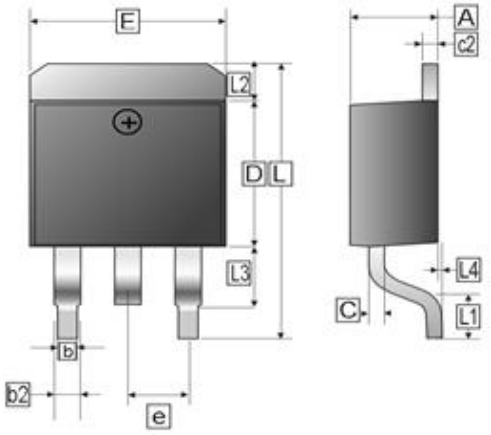

REF.	Millimeter	
	Min.	Max.
A	4.00	4.87
b	0.508	1.01
L4	0	0.30
C	0.30	0.74
L3	1.50 REF.	
L1	2.50 REF.	
E	9.60	10.67
c2	1.07	1.65
b2	1.34 REF.	
D	8.00	9.652
e	2.54 REF.	
L	14.6	16.1
L2	1.27 REF.	

MOUNTING PAD LAYOUT

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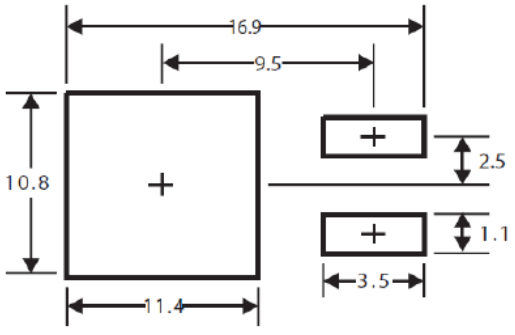

*Dimensions in millimeters