Elektronische Bauelemente

# STT3962N

**N-Channel Enhancement Mode Mos.FET**

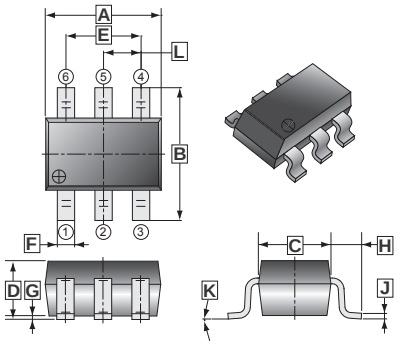
**2.3 A, 60 V, $R_{DS(ON)}$ 0.153 Ω**

RoHS Compliant Product
A suffix of "-C" specifies halogen and lead-free

## DESCRIPTION

These miniature surface mount MOSFETs utilize High Cell Density process. Low $R_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are DC-DC converters, power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

**TSOP-6**



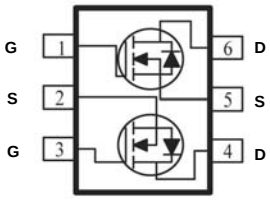

## FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Miniature TSOP-6 surface mount package saves board space.

## PRODUCT SUMMARY

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$(V) | $R_{DS}$(on) (Ω) | $I_D$(A) |
| 60 | 0.153@$V_{GS}$= 10V | 2.3 |
| | 0.185@$V_{GS}$= 4.5V | 2.1 |

| REF. | Millimeter | | REF. | Millimeter | |
|---|---|---|---|---|---|
| | Min. | Max. | | Min. | Max. |
| A | 2.70 | 3.10 | G | 0 | 0.10 |
| B | 2.60 | 3.00 | H | 0.60 REF. | |
| C | 1.40 | 1.80 | J | 0.12 REF. | |
| D | 1.10 MAX. | | K | 0° | 10° |
| E | 1.90 REF. | | L | 0.95 REF. | |
| F | 0.30 | 0.50 | | | |




## ABSOLUTE MAXIMUM RATINGS($T_A$=25°C UNLESS OTHERWISE NOTED)

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| | | Maximum | |
| Drain-Source Voltage | $V_{DS}$ | 60 | V |
| Gate-Source Voltage | $V_{GS}$ | ±20 | V |
| Continuous Drain Current [a] | $I_D$ @TA=25℃ | 2.3 | A |
| | $I_D$ @TA=70℃ | 1.9 | |
| Pulsed Drain Current [b] | $I_{DM}$ | 8 | A |
| Continuous Source Current (Diode Conduction) [a] | $I_S$ | 1.05 | A |
| Power Dissipation [a] | $P_D$ @TA=25℃ | 1.15 | W |
| | $P_D$ @TA=70℃ | 0.7 | |
| Operating Junction and Storage Temperature Range | Tj, Tstg | -55 ~ 150 | °C |

| THERMAL RESISTANCE RATINGS | | | | |
|---|---|---|---|---|
| Parameter | | Symbol | Maximum | Unit |
| Maximum Junction to Ambient [a] | t ≦ 10 sec | $R_{\theta JA}$ | 100 | °C / W |
| | Steady State | | 166 | |

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature.

## ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Gate-Threshold Voltage | $V_{GS(th)}$ | 1 | - | - | V | $V_{DS}$=$V_{GS}$, $I_D$= 250uA |
| Gate-Body Leakage Current | $I_{GSS}$ | - | - | 100 | uA | $V_{DS}$= 0V, $V_{GS}$= 20V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | - | - | 1 | uA | $V_{DS}$= 48V, $V_{GS}$= 0V |
| | | - | - | 10 | | $V_{DS}$= 48V, $V_{GS}$=0 V, $T_J$= 55°C |
| On-State Drain Current [a] | $I_{D(on)}$ | 5 | - | - | A | $V_{DS}$ = 5V, $V_{GS}$= 10 V |
| Drain-Source On-Resistance [a] | $R_{DS(ON)}$ | - | - | 0.153 | Ω | $V_{GS}$= 10V, $I_D$= 2.3A |
| | | - | - | 0.185 | | $V_{GS}$= 4.5V, $I_D$= 2.1A |
| Forward Transconductance [a] | $g_{fs}$ | - | 10 | - | S | $V_{DS}$= 5V, $I_D$= 2.3A |
| Diode Forward Voltage [a] | $V_{SD}$ | - | 0.80 | - | V | $I_S$= 1.05A, $V_{GS}$= 0V |
| **DYNAMIC [b]** | | | | | | |
| Total Gate Charge | $Q_g$ | - | 3 | - | nC | $V_{DS}$= 15V, $V_{GS}$= 4.5V, $I_D$= 2.3A |
| Gate-Source Charge | $Q_{gs}$ | - | 0.6 | - | | |
| Gate-Drain Charge | $Q_{gd}$ | - | 1.0 | - | | |
| Turn-on Delay Time | $T_{d(on)}$ | - | 5 | - | nS | $V_{DD}$= 15V, $V_{GS}$= 4.5V, $R_{GEN}$= 15Ω, $I_D$= 1A |
| Rise Time | $T_r$ | - | 12 | - | | |
| Turn-off Delay Time | $T_{d(off)}$ | - | 13 | - | | |
| Fall Time | $T_f$ | - | 7 | - | | |

Notes

a. Pulse test : PW ≦ 300 us duty cycle ≦ 2%.

b. Guaranteed by design, not subject to production testing.

## CHARACTERISTIC CURVES

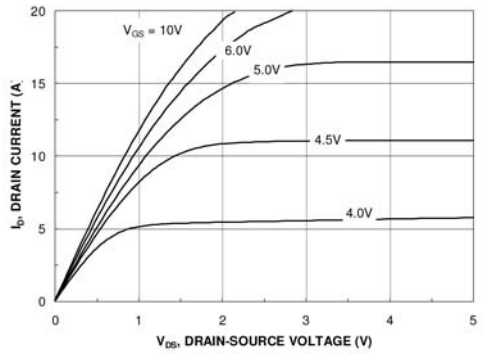



Figure 1. On-Region Characteristics.

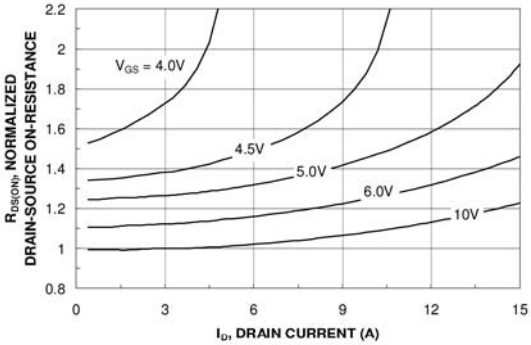



Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

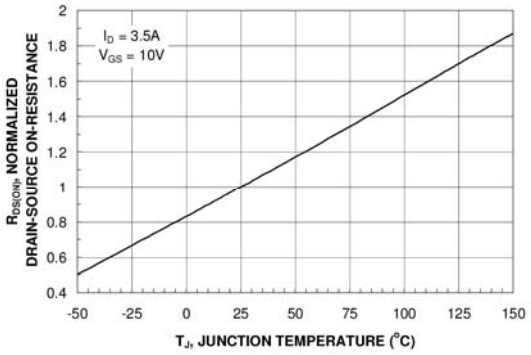



Figure 3. On-Resistance Variation withTemperature.

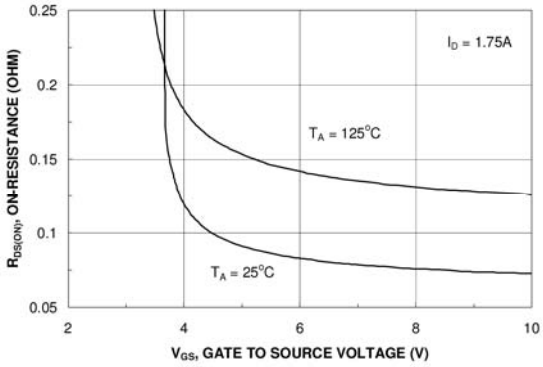
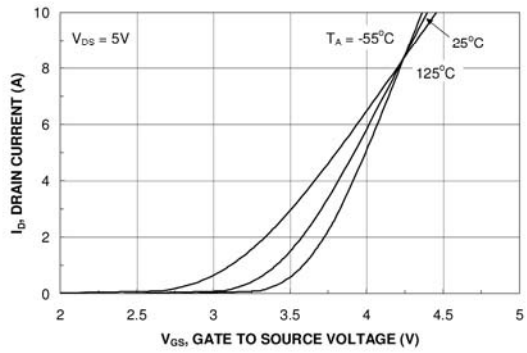
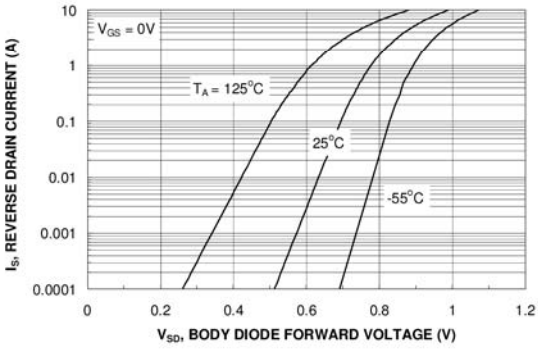



Figure 4. On-Resistance Variation with Gate-to-Source Voltage.



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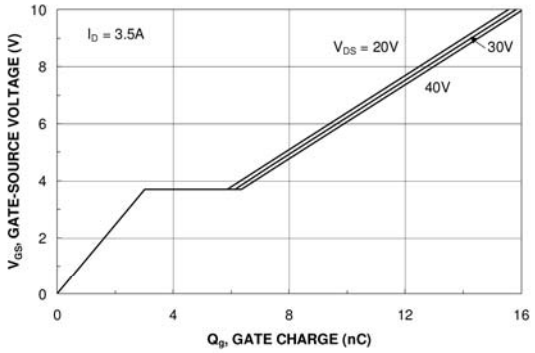


Figure 7. Gate Charge Characteristics.

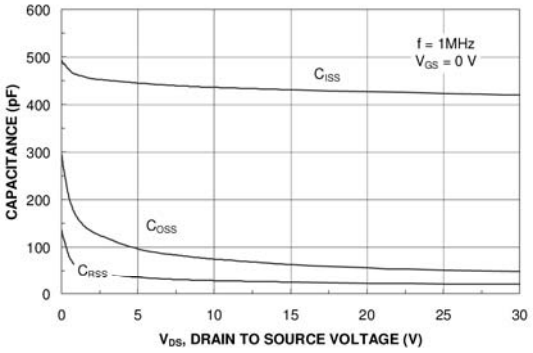


Figure 8. Capacitance Characteristics.

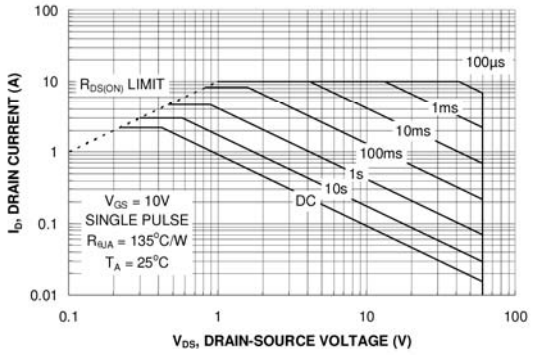


Figure 9. Maximum Safe Operating Area.

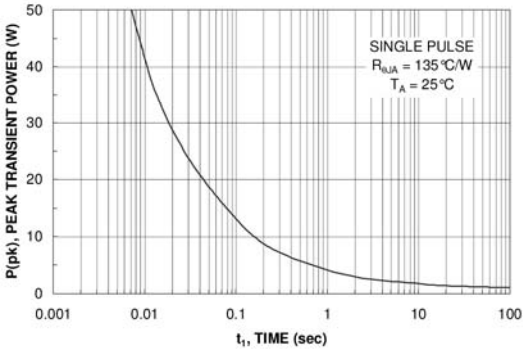


Figure 10. Single Pulse Maximum Power Dissipation.

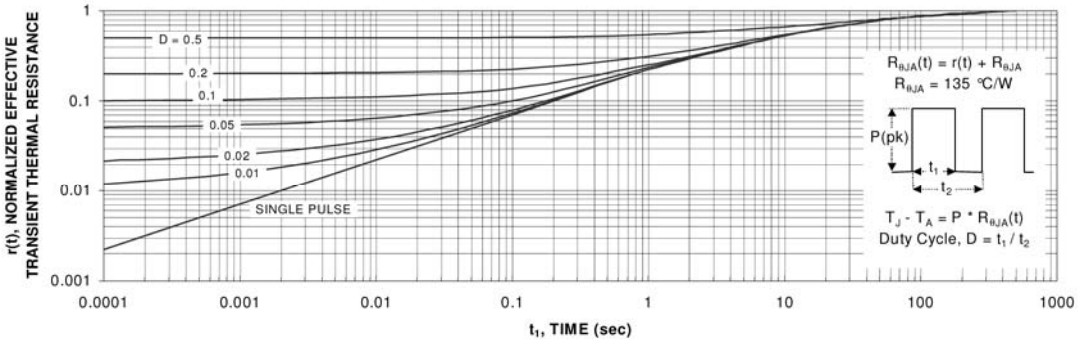


Figure 11. Transient Thermal Response Curve.
Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.