

RoHS Compliant Product

A suffix of "-C" specifies halogen & lead-free

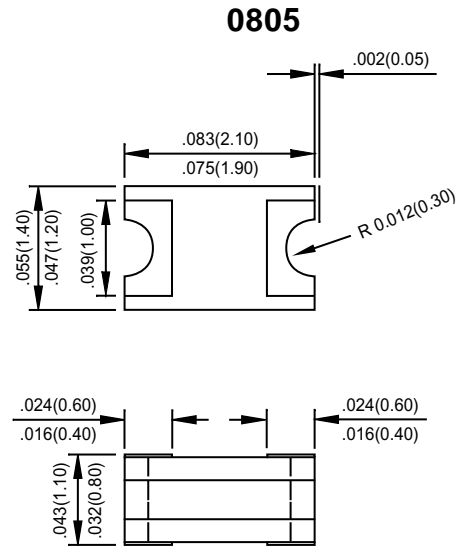


FEATURES

- * Plastic package has Underwriters Laboratory Flammability
- * Classification 94V-0
- * Low profile package
- * Built-in strain relief
- * Metal to silicon rectifier , majority carrier conduction
- * Low power loss , High efficiency
- * High current capability
- * High surge capacity
- For using in low voltage high frequency switching power supply, inverters , free wheeling , and polarity protection applications

MECHANICAL DATA

- * Case : Packed with FRP substrate and epoxy underfilled
- * Terminals : Solder plated , solderable per MIL-STD-750, Method 2026
- * Polarity : Laser marking
- * Weight : 0.005 gram
- * Marking: MSCD104 = A4



*Dimensions in inches and (millimeters)

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Rating 25°C ambient temperature unless otherwise specified. Single phase half wave, 60Hz, resistive or inductive load. For capacitive load, derate current by 20%.

TYPE NUMBER	SYMBOLS	MSCD104	Unit
Maximum Recurrent Peak Reverse Voltage	V_{RRM}	40	V
Working Peak Reverse Voltage	V_{RMS}	40	V
Maximum DC Blocking Voltage	V_{DC}	40	V
Maximum Average Forward Rectified Current (See FIG. 1)	$I_{(AV)}$	1	A
Peak Forward Surge Current, 8.3 ms single half sine-wave superimposed on rated load (JEDEC method)	I_{FSM}	3	A
Maximum Instantaneous Forward Voltage at 1.0A (Note1)	V_F	0.52	V
Maximum DC Reverse Current (Note1) $T_a=25$ at Rated DC Blocking Voltage $T_a=100$	I_R	0.1	mA
		5	
Typical Thermal Resistance (Note 2)	$R_{\theta JA}$	88	°C / W
	$R_{\theta JL}$	28	
Operating Temperature Range	T_J	-50 ~ +125	°C
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

NOTES:

1. Pulse test width PW=300 usec, 1% duty cycle.
2. Mounted on P.C. board with 0.2 x 0.2" (5.0 x 5.0mm) copper pad areas.

FIG. 1 - TYPICAL FORWARD CURRENT DERATING CURVE

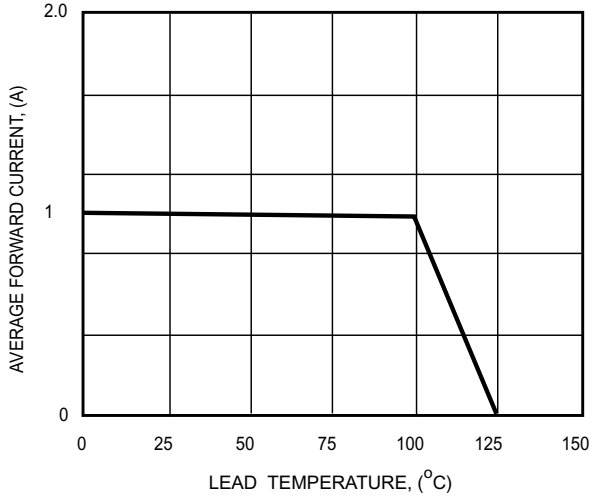


FIG.2 - MAXIMUM NON-REPETITIVE PEAK FORWARD SURGE CURRENT

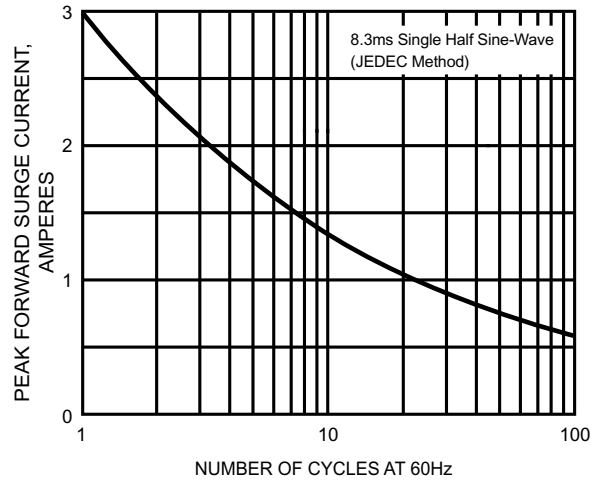


FIG. 3 - FORWARD CHARACTERISTICS

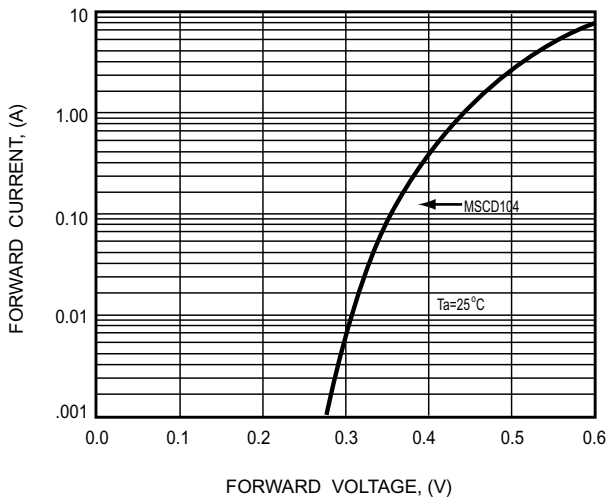


FIG. 4 - REVERSE CHARACTERISTICS

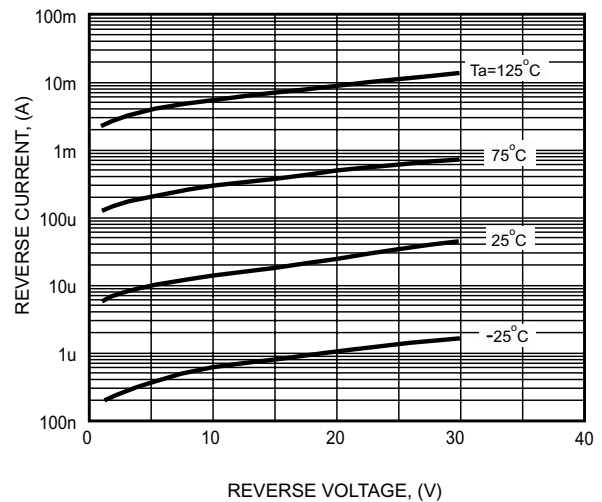


FIG. 5 - TYPICAL JUNCTION CAPACITANCE

